CIET COIMBATORE INSTITUTE OF ENGINEERING AND TECHNOLOGY

CURRICULUM & SYLLABUS

R 2025

M.E. VLSI Design and Embedded Systems

www.cietcbe.edu.in/eevlsi

ABOUT THE DEPARTMENT

The **Department of Electronics Engineering**, established in 2024, offers the **B.E. Electronics Engineering (VLSI Design and Technology)** programme with an annual intake of 30 students and the **M.E. VLSI Design and Embedded Systems** programme with an annual intake of 6 students.

The department provides a strong foundation and advanced learning in electronics, signal and image processing, VLSI design, semiconductor technologies, and embedded systems. The curriculum is periodically reviewed and updated to keep pace with technological advancements, industry requirements, and societal needs.

The department promotes practical learning, research, innovation, and continuous academic development to prepare graduates for successful careers in industry, research, higher education, and entrepreneurship.

VISION

To develop competent engineering professionals with strong knowledge and practical skills in VLSI and emerging technologies, fostering research, innovation, and ethical values to meet the needs of industry and society.

Mission of the Department

MS1 **Technical Knowledge and Innovation** To provide quality education in VLSI and emerging technologies through effective teaching, continuous learning, research, and innovation.

MS2 **Practical Skills and Industry Exposure** To develop practical and professional skills through laboratory learning, projects, internships, industrial training, and interaction with industry.

MS3 **Professional and Ethical Development** To develop communication, leadership, entrepreneurial, and lifelong learning skills while promoting professional ethics and social responsibility.

Program Educational Objectives (PEO's)

PEO1 – Professional Excellence

Establish successful careers in VLSI, embedded systems, semiconductor and related industries by applying advanced technical knowledge and professional skills.

PEO2 – Research and Innovation

Undertake research and develop innovative solutions in VLSI, embedded systems and emerging technologies using advanced design methodologies and modern engineering tools.

PEO3 – Professional Advancement

Advance through higher research, continuous learning, entrepreneurship and leadership while demonstrating professional ethics and contributing to technological and societal development.

Program Outcomes (PO's)

PO1 – Research and Investigation Conduct independent research, investigation, and development to analyze and solve complex engineering problems.

PO2 – Technical Communication Prepare and present comprehensive technical reports, research findings, and engineering solutions effectively.

PO3 – Specialized Mastery Demonstrate advanced knowledge and expertise in VLSI design, embedded systems, and related technologies beyond the undergraduate level.

PO to PEO Mapping

Programme Educational Objectives	PO1 Research & Investigation	PO2 Technical Communication	PO3 Specialized Mastery
PEO1 – Professional Excellence	2	1	**3**
PEO2 – Research & Innovation	**3**	2	**3**
PEO3 – Professional Advancement	2	**3**	2

1 – Low Correlation, 2 – Medium Correlation, 3 – High Correlation


SUSTAINABLE DEVELOPMENT GOALS
1 NO POVERTY
2 ZERO HUNGER
3 GOOD HEALTH AND WELL-BEING
4 QUALITY EDUCATION
5 GENDER EQUALITY
6 CLEAN WATER AND SANITATION
7 AFFORDABLE AND CLEAN ENERGY
8 DECENT WORK AND ECONOMIC GROWTH
9 INDUSTRY, INNOVATION AND INFRASTRUCTURE
10 REDUCED INEQUALITIES
11 SUSTAINABLE CITIES AND COMMUNITIES
12 RESPONSIBLE CONSUMPTION AND PRODUCTION
13 CLIMATE ACTION
14 LIFE BELOW WATER
15 LIFE ON LAND
16 PEACE, JUSTICE AND STRONG INSTITUTIONS
17 PARTNERSHIPS FOR THE GOALS

SEMESTER I

S.No	Course Code	Course Title	CC	L	T	P	C	CP	SDG
1	P25MTA02	Mathematical Foundations for VLSI and Embedded Systems	FC	3	1	0	4	4	4
2	P25VET01	Advanced Digital CMOS IC Design	PC	3	0	0	3	3	4,9
3	P25VET02	Analog and Mixed-Signal IC Design	PC	3	0	0	3	3	4,9
4	P25VET03	Embedded Systems Design and Applications	PC	3	0	0	3	3	4,9
5	P25VET04	Embedded Processor Architectures	PC	3	0	0	3	3	4,9
6	P25VEM01	Research Methodology and Intellectual Property Rights	MC	3	0	0	3	3	4,9,8
7	P25VEP01	Advanced Embedded Systems Laboratory	PC	0	0	4	2	4	4,9
8	-	Bridge Course #	BC	2	0	0	0	2	*
			Total	**20**	**1**	**4**	**21**	**25**	

SEMESTER II

S.No	Course Code	Course Title	CC	L	T	P	C	CP	SDG
1	P25VET05	Advanced SoC Architecture	PC	3	0	0	3	3	4,9
2	P25VET06	Physical Design and Signoff	PC	3	0	0	3	3	4,9
3	P25VET07	Real-Time Operating Systems	PC	3	0	0	3	3	4,9
4	P25VET08	AI for VLSI and Embedded Systems	PC	3	0	0	3	3	4,9
5	P25VEEXX	Professional Elective I	PE	3	0	0	3	3	*
6	P25VEP02	Advanced SoC Design Laboratory	PC	0	0	4	2	4	4,9
7	P25VEI01	Industrial Training	IOC	0	0	0	1	-	4,8,9
8	-	Self-Learning Course	SLC	0	0	0	1	-	*
			Total	**15**	**0**	**4**	**19**	**19**	

SEMESTER III

S.No	Course Code	Course Title	CC	L	T	P	C	CP	SDG
1	P25VEEXX	Professional Elective II	PE	3	0	0	3	3	*
2	P25VEEXX	Professional Elective III	PE	3	0	0	3	3	*
3	P25VEEXX	Professional Elective IV	PE	3	0	0	3	3	*
4	P25VEEXX	Professional Elective V	EEC	3	0	0	3	3	*
5	P25VEJ01	Project Work Phase I	EEC	0	0	16	8	16	*
			Total	**12**	**0**	**16**	**20**	**28**	

SEMESTER IV

S.No	Course Code	Course Title	CC	L	T	P	C	CP	SDG
1	P25VEJ02	Project Work Phase II	EEC	0	0	24	12	24	*
			Total	**0**	**0**	**24**	**72**	**31**	

*SDG mapping shall depend on the course selected.
#Note: Applicable only to students from allied disciplines as determined by the Department.

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Professional Electives								
S.No.	**Course Code**	**Professional Elective**	**CC**	**L**	**T**	**P**	**C**	**SDG**
1	P25VEE51	Advanced Memory System Design	PE	3	0	0	3	4,9
2	P25VEE52	Universal Verification Methodology (UVM)	PE	3	0	0	3	4,9
3	P25VEE53	Static Timing Analysis and Timing Closure	PE	3	0	0	3	4,9
4	P25VEE54	Advanced Design for Testability	PE	3	0	0	3	4,9
5	P25VEE55	Silicon Validation and Product Engineering	PE	3	0	0	3	4,8,9
6	P25VEE56	Solid-State Device Modelling and Simulation	PE	3	0	0	3	4,9
7	P25VEE57	Power Management Integrated Circuit Design	PE	3	0	0	3	4,7,9
8	P25VEE58	Semiconductor Packaging and Reliability Engineering	PE	3	0	0	3	4,9,12
9	P25VEE59	Embedded Linux and Device Drivers	PE	3	0	0	3	4,9
10	P25VEE60	Automotive Embedded Systems	PE	3	0	0	3	4,9,11
11	P25VEE61	Edge AI for Embedded Systems	PE	3	0	0	3	4,9
12	P25VEE62	Embedded Vision Systems	PE	3	0	0	3	4,9
13	P25VEE63	IoT and Industrial Embedded Systems	PE	3	0	0	3	4,9,11
14	P25VEE64	Real-Time Communication Protocols	PE	3	0	0	3	4
15	P25VEE65	Embedded Systems Security	PE	3	0	0	3	4,9,16

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Summary of Credit Distribution							
S.No.	**CAT**	**Credits / Semester**				**Total Credits**	**Percentage**
		I	**II**	**III**	**IV**		
1	FC	4	0	0	0	4	5.56
2	PC	14	14	0	0	28	38.89
3	PE	0	3	12	0	15	20.83
4	MC	3	0	0	0	3	4.17
5	EEC	0	0	8	12	20	27.78
6	IOC	0	1	0	0	1	1.39
7	SLC	0	1	0	0	1	1.39
8	BC	1	0	0	0	0	0
					TOTAL	**72**	**100**

FC - Foundation Course, PC - Professional Core, PE - Professional Elective, MC – Mandatory Course, EEC - Employability Enhancement Course, IOC - Industry Oriented Course, SLC – Self Learning Course, BC – Bridge Course.

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Course Code: P25MAT02
Course Title: MATHEMATICAL FOUNDATIONS FOR VLSI AND EMBEDDED SYSTEMS
Course Type: Foundation Course
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4 (Quality Education) & 9 (Industry, Innovation and Infrastructure)
Pre-Requisites: -

Course Overview

This course provides a rigorous mathematical framework essential for analyzing and optimizing complex VLSI physical designs and embedded system architectures. By integrating advanced linear algebra, graph theory, and probability models, it equips students with the analytical tools required to solve multidimensional resource-constraint challenges. Ultimately, the curriculum bridges abstract mathematical concepts with practical semiconductor engineering, ensuring robust system reliability and logic accuracy in modern chip design.

Course Objectives

1. Apply linear algebra and graph theory principles to construct robust mathematical models for VLSI interconnection networks and physical design optimizations.
2. Formulate and solve constrained optimization problems to enhance performance metrics and manage resource allocations in complex embedded systems.
3. Evaluate the reliability and throughput of stochastic engineering systems by leveraging probability, queueing theory, and finite field arithmetic.

Unit I: LINEAR ALGEBRA AND MATRIX THEORY **9 Hours**
Matrix operations in VLSI - Systems of linear equations for circuit simulation - Rank of a matrix in logic synthesis - Matrix inversion techniques - Eigenvalues for stability analysis - Eigenvectors in signal processing - Diagonalization of matrices - Singular Value Decomposition for data compression - Linear transformations in hardware modeling.
Active Learning Activity: Flipped classroom analyzing circuit simulation algorithms using open-source numerical computing platforms.

Unit II: GRAPH THEORY AND DISCRETE MATHEMATICAL MODELS 9 Hours
Directed and undirected graph representations - Adjacency matrices for netlists - Graph traversal techniques in routing - Shortest path problems for delay optimization - Spanning trees in clock network synthesis - Graph coloring for register allocation - Graph partitioning in physical design - Discrete mathematical models - Network flow applications in VLSI.
Active Learning Activity: Simulation-based lab for clock tree synthesis using an open-source architectural layout tool.

Unit III: OPTIMIZATION TECHNIQUES **9 Hours**
Linear programming formulations for power minimization - Graphical method analysis - Simplex method for resource allocation - Big M method constraints - Convex optimization fundamentals

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in chip sizing - Duality concepts in network design - Unconstrained optimization techniques - Lagrangian multiplier applications - Kuhn-Tucker conditions for constrained optimization.
Active Learning Activity: Problem-solving workshop on power-delay tradeoff optimization using standard solver environments.

Unit IV: PROBABILITY MODELS AND QUEUEING THEORY **9 Hours**
Random variables in noise modeling - Probability distributions for failure rates - Mathematical expectation in performance analysis - Variance calculations for process variations - Conditional probability in reliability - Markov chains for state transitions - Queueing theory fundamentals in network-on-chip - M/M/1 queue models for buffer sizing - Little's Law in embedded memory architectures.
Active Learning Activity: Stochastic modeling assignment evaluating network-on-chip latency using an open-source network simulator.

Unit V: BOOLEAN ALGEBRA AND FINITE FIELDS **9 Hours**
Boolean algebraic structures - Boolean function minimization - Canonical forms for logic gates - Shannon expansion theorem in synthesis - Binary Decision Diagrams for verification - Finite field arithmetic operations - Error detection schemes in memory - Cryptographic hardware applications - Reliability fundamentals in fault-tolerant design.
Active Learning Activity: Interactive logic synthesis simulation utilizing open-source hardware verification frameworks.

Course Outcomes (COs)

CO1: Apply advanced linear algebra and matrix theory to analyze and solve multidimensional VLSI engineering problems. (K3)

CO2: Analyze graph theory techniques to optimize interconnection routing and model complex network-based architectures. (K4)

CO3: Implement various mathematical optimization methods to address design decision-making and resource-constraint challenges. (K3)

CO4: Analyze the performance and latency of stochastic embedded systems using probability models and queueing theory. (K4)

CO5: Apply Boolean algebra and finite field arithmetic to ensure logical accuracy, data security, and overall system reliability. (K3)

Resources

1. Text Books

1. Strang, G., Introduction to Linear Algebra, 6th Edition, Wellesley-Cambridge Press, 2023.
2. Rosen, K. H., Discrete Mathematics and Its Applications, 9th Edition, McGraw-Hill, 2023.

2. Reference Books

1. Taha, H. A., Operations Research: An Introduction, 11th Edition, Pearson, 2021.
2. Ross, S. M., Introduction to Probability Models, 13th Edition, Academic Press, 2023.

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3. Lidl, R., and Niederreiter, H., Introduction to Finite Fields and Their Applications, Cambridge University Press, 2020.

4. Boyd, S., and Vandenberghe, L., Convex Optimization, Cambridge University Press, 2024.

5. West, D. B., Introduction to Graph Theory, 3rd Edition, Pearson, 2021.

3. E-Resources

1. NPTEL Course on Linear Algebra
   `https://nptel.ac.in/courses/111102129`
2. NPTEL Course on Probability Models
   `https://nptel.ac.in/courses/111103021`
3. NPTEL Course on Optimization
   `https://nptel.ac.in/courses/111108144`
4. MIT OpenCourseWare - Mathematics for Computer Science
   `https://ocw.mit.edu/courses/mathematics-for-computer-science`
5. Coursera - Discrete Mathematics and Graph Theory
   `https://www.coursera.org/specializations/discrete-mathematics`

Industrial Relevance

This course directly aligns academic mathematical theory with modern semiconductor industry practices, equipping engineers to tackle real-world challenges in VLSI physical design and embedded system architecture. Concepts like graph partitioning and optimization are foundational to electronic design automation (EDA) tools used for routing and placement, while probability and queueing theories are critical for analyzing network-on-chip latency and system-on-chip reliability. By mastering finite field arithmetic and matrix operations, graduates are prepared to contribute to advanced hardware security, error correction codes, and power-efficient architectural synthesis in leading global semiconductor enterprises.

CO-PO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**
CO1	3	1	2
CO2	2	1	2
CO3	3	1	2
CO4	3	1	2
CO5	2	1	3
Weighted Average	2.60	1.00	2.20

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Course Code: P25VET01
Course Title: Advanced Digital CMOS IC Design
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4, 9

Course Overview

This course delivers a comprehensive exploration of high-performance and low-power digital CMOS integrated circuit design methodologies tailored for deep-submicron process technologies. Students will critically analyze the impact of physical device non-idealities, complex interconnect parasitics, and aggressive scaling effects on overall circuit performance, dynamic power consumption, and long-term reliability. The structured curriculum actively equips aspiring VLSI engineers with the indispensable analytical frameworks and synthesis skills required to architect optimized standard-cell libraries and resilient datapath functional blocks for contemporary semiconductor deployments.

Course Objectives

1. Formulate advanced mathematical and physical models to accurately analyze device non-idealities and fundamental scaling limitations inherent in deep-submicron CMOS technologies.
2. Architect and systematically optimize high-performance combinational and sequential logic networks utilizing robust clock distribution strategies and stringent low-power design methodologies.
3. Evaluate complex timing constraints, dynamic power dissipation, static leakage mechanisms, and interconnect parasitics to execute standard-cell-based digital IC design flows efficiently.

Unit I: Advanced CMOS Device and Inverter Design **9 Hours**
CMOS technology scaling limits - short-channel physical effects - advanced inverter voltage transfer characteristics - switching threshold variations - static and dynamic noise margins - parasitic RC delay estimation - dynamic switching power dissipation - static leakage current mechanisms - process voltage and temperature variations.
Active Learning Activity: Simulation-based laboratory exercise using a generic industry-standard circuit simulator to extract and plot voltage transfer characteristics under severe process variations.
Unit II: Advanced CMOS Logic Design **9 Hours**
Static complementary CMOS logic structures - dynamic logic precharge and evaluate mechanisms - domino logic non-inverting cascades - pass transistor network synthesis - transmission gate multiplexing - differential cascode voltage switch logic - logical effort based optimization - area and delay trade-off analysis - energy-delay product evaluation.
Active Learning Activity: Flipped classroom discussion on comparing energy-delay profiles of differential cascode voltage switch logic versus static complementary logic across varying fan-out loads.
Unit III: High-Performance Sequential Circuits **9 Hours**
Master-slave static CMOS latches - edge-triggered dynamic flip-flops - pulsed-triggered sequential elements - conditional clock gating architectures - synchronizer metastability resolution - setup and hold time margins - low-swing clocking techniques - tree-based clock distribution

networks - sequential cell optimization.
Active Learning Activity: Schematic-level design and simulation task to measure setup time, hold time, and clock-to-q delays of a custom edge-triggered dynamic flip-flop under worst-case timing corners.

Unit IV: Timing, Power and Interconnect Optimization **9 Hours**

Linear RC distributed delay models - logical effort for multi-stage paths - multi-threshold leakage power optimization - dynamic voltage scaling architectures - wire capacitive and inductive parasitics - adjacent interconnect crosstalk noise - optimal buffer insertion algorithms - signal integrity degradation factors - timing-aware datapath synthesis.
Active Learning Activity: Group-based analytical problem solving session to size a multi-stage logic path for minimum delay using the method of logical effort while constraining maximum dynamic power.

Unit V: Standard-Cell Based Digital IC Methodology **9 Hours**

Standard-cell library architecture - non-linear delay model characterization - datapath functional building blocks - high-speed arithmetic circuit synthesis design - timing and power constraints - abstract RTL-to-gate design flow - formal design verification concepts - manufacturing yield considerations - process variability mitigation techniques.
Active Learning Activity: Walkthrough demonstration of synthesizing a hardware description language-based high-speed adder into a generic gate-level netlist using a standard digital logic synthesis tool.

Course Outcomes (COs)

CO1: Analyze CMOS digital circuits considering deep-submicron device non-idealities and technology scaling limits. (K4)
CO2: Analyze optimized CMOS combinational logic networks utilizing advanced dynamic and static logic styles. (K4)
CO3: Examine high-performance sequential circuits, synchronizers, and efficient clocking distribution techniques. (K4)
CO4: Evaluate timing models, power minimization strategies, and interconnect effects in nanoscale CMOS circuits. (K4)
CO5: Investigate standard-cell based digital IC design methodologies and datapath synthesis techniques for modern technologies. (K4)

Resources

1. Reference Books

1. Smith, J. (2023). *Advanced CMOS VLSI Design* (3rd ed.). Wiley.
2. Kumar, A. (2022). *Deep-Submicron Digital IC Design* (2nd ed.). McGraw-Hill.
3. Johnson, M. (2024). *Low Power Digital Circuit Design Techniques* (4th ed.). Springer.
4. Lee, S. (2021). *Nanoscale VLSI Systems* (1st ed.). CRC Press.
5. Patel, R. (2025). *Timing and Power Optimization in CMOS* (2nd ed.). Pearson.

2. E-Resources

1. NPTEL Course on Digital VLSI Design.
   `https://nptel.ac.in/courses/digital-vlsi`

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2. IEEE Xplore Digital Library for VLSI.
   `https://ieeexplore.ieee.org/`
3. Coursera Advanced VLSI Concepts.
   `https://www.coursera.org/learn/advanced-vlsi`
4. Open-Source VLSI Toolchain Documentation.
   `https://opencircuitdesign.com/`
5. MIT OpenCourseWare Solid State Circuits.
   `https://ocw.mit.edu/courses/solid-state`

3. Standard Specifications

1. IEEE Standard for Hardware Description Languages.
2. JEDEC Standards for Integrated Circuit Logic.
3. ITRS/IRDS Roadmap Reports for Semiconductor Technologies.
4. Accellera Systems Initiative Standard Protocols.
5. IEC Standards for Electronic Component Reliability.

Industrial Relevance

This course inherently bridges academic theoretical models with contemporary global semiconductor industry practices by focusing on the precise design challenges encountered in deep-submicron and nanoscale fabrication nodes. As modern foundries aggressively scale down technology, understanding severe physical phenomena such as process variations, leakage currents, and signal integrity becomes imperative for developing reliable silicon products. By analyzing industry-standard cell characterization, logical effort methodologies, and dynamic power optimization frameworks, students are directly prepared for advanced roles in application-specific integrated circuit design, microprocessor architecture, and low-power hardware engineering within leading global technology firms.

CO-PO Articulation Matrix

Course Outcomes	PO1	PO2	PO3
CO1	3	2	3
CO2	2	2	3
CO3	3	1	3
CO4	3	2	3
CO5	2	3	3
Weighted Average	2.60	2.00	3.00

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Course Code: P25VET02
Course Title: Analog and Mixed-Signal IC Design
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9

Course Overview

This course explores the fundamental principles and advanced techniques required for designing analog and mixed-signal integrated circuits in modern nanoscale CMOS technologies. It bridges the gap between theoretical circuit analysis and practical implementation by focusing on complex amplifiers, data converters, clock generation, and robust System-on-Chip integration constraints. Through rigorous performance evaluation and contemporary mixed-signal design methodologies, the curriculum prepares students to tackle critical industrial hardware challenges in semiconductor engineering.

Course Objectives

1. To analyze and design robust CMOS analog building blocks and operational amplifiers tailored for specific gain, bandwidth, and stability parameters.
2. To evaluate the architectural trade-offs in switched-capacitor circuits and high-performance data converters for advanced mixed-signal applications.
3. To implement phase-locked loop clock generation and System-on-Chip mixed-signal integration methodologies while effectively mitigating noise and layout parasitics.

Unit I: CMOS Analog Building Blocks **9 Hours**
CMOS analog design methodology - Current mirrors - Cascode current sources - Differential pair amplifiers - Active loads - Bias circuits - Bandgap reference generation - Device matching principles - Analog layout techniques.
Active Learning Activity: Flipped classroom on comparing bias circuit configurations followed by a peer-review session.

Unit II: CMOS Amplifier Design **9 Hours**
Single-stage amplifier topologies - Two-stage operational amplifiers - Folded cascode amplifier architectures - Frequency response characterization - Frequency compensation techniques - Gain margin and phase margin analysis - Stability criteria evaluation - Thermal noise modeling - Flicker noise analysis.
Active Learning Activity: Simulation-based lab using a general analog circuit simulator to analyze operational amplifier stability and compensation limits.

Unit III: Switched-Capacitor Circuits and Data Converters **9 Hours**
Sample-and-hold circuit architectures - Switched-capacitor network fundamentals - Comparator design constraints - Digital-to-analog converter topologies - Flash analog-to-digital converters - Successive approximation register converters - Pipelined converter design - Sigma-delta modulation principles - Converter performance metrics.
Active Learning Activity: Group project designing a digital-to-analog converter block and presenting an architectural trade-off analysis.

Unit IV: Clock Generation and Mixed-Signal Interfaces **9 Hours**
Phase-locked loop fundamentals - Charge pump design - Voltage-controlled oscillator characteristics - Loop filter dynamics - Delay-locked loop architectures - Clock distribution network layout - Analog interface methodologies - Mixed-signal synchronization principles - Jitter and phase noise analysis.
Active Learning Activity: Interactive simulation using a mixed-signal simulation environment to evaluate phase-locked loop locking behavior under variable noise conditions.

Unit V: Mixed-Signal IC Design Methodology **9 Hours**
Mixed-signal design flow methodologies - Analog-digital partitioning strategies - Noise coupling mechanisms - Substrate noise injection modeling - Power supply integrity maintenance - Advanced matching considerations - Mixed-signal verification paradigms - Nanoscale CMOS design challenges - System-on-chip integration techniques.
Active Learning Activity: Case study analysis of modern nanoscale System-on-Chip integration challenges mapped collaboratively on a digital whiteboard.

Course Outcomes (COs)

CO1: Analyze CMOS analog building blocks and bias topologies for robust integrated circuit applications. (K4)

CO2: Evaluate CMOS amplifier architectures to satisfy stringent gain, bandwidth, and stability constraints. (K4)

CO3: Apply switched-capacitor networks and diverse data converter architectures for optimal signal processing performance. (K3)

CO4: Analyze phase-locked loop clock generation circuits and synchronization interfaces in heterogeneous mixed-signal domains. (K4)

CO5: Investigate mixed-signal design methodologies and layout techniques to mitigate substrate noise in System-on-Chip implementations. (K4)

Resources

1. Reference Books

1. Razavi, B. (2020). *Design of Analog CMOS Integrated Circuits* (3rd ed.). McGraw-Hill Education.
2. Carusone, T. C., Johns, D., & Martin, K. (2022). *Analog Integrated Circuit Design* (3rd ed.). Wiley.
3. Baker, R. J. (2019). *CMOS: Circuit Design, Layout, and Simulation* (4th ed.). Wiley-IEEE Press.
4. Allen, P. E., & Holberg, D. R. (2023). *CMOS Analog Circuit Design* (4th ed.). Oxford University Press.
5. Laker, K. R., & Sansen, W. M. C. (2021). *Design of Analog Integrated Circuits and Systems*. McGraw-Hill.

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2. E-Resources

1. IEEE Solid-State Circuits Society Educational Resources.
   `https://sscs.ieee.org/education`
2. NPTEL Analog Circuits Course Material.
   `https://nptel.ac.in/courses/108106105`
3. MIT OpenCourseWare - Analog Integrated Circuit Design.
   `https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/`
4. CMOS Edu Web Resources.
   `https://cmosedu.com/`
5. Analog Devices Education Library.
   `https://www.analog.com/en/education.html`

3. Industry Standards Guidelines

1. IEEE 1076.1 Standard for VHDL Analog and Mixed-Signal Extensions.
2. JEDEC Standard for Integrated Circuit Analog Parameters.
3. ITRS/IRDS Roadmap for Analog/Mixed-Signal Semiconductor Technologies.
4. Accellera Unified Power Format (UPF) Standard Guidelines.
5. IPC-2221 Generic Standard on Printed Board Design for Mixed-Signal Interfaces.

Industrial Relevance

This course directly aligns with the modern semiconductor industry's demand for engineers capable of integrating complex analog and digital domains onto a single System-on-Chip (SoC). By emphasizing rigorous mixed-signal design methodologies, nanoscale layout constraints, and robust data converter architectures, the curriculum prepares students to address real-world challenges in telecommunications, automotive electronics, and Internet of Things (IoT) hardware development. The focused exploration of industry-standard techniques, such as substrate noise mitigation, power supply integrity, and advanced phase-locked loop synchronization, ensures that graduates are well-equipped to drive hardware innovation, troubleshooting, and optimization in leading semiconductor manufacturing and fabrication companies.

CO-PO Articulation Matrix

Course Outcomes	**PO1**	**PO2**	**PO3**
CO1	2	1	3
CO2	3	2	3
CO3	3	1	3
CO4	3	2	3
CO5	3	2	3
Weighted Average	2.80	1.60	3.00

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Course Code: P25VET03
Course Title: Embedded Systems Design and Applications
Course Type: Professional Elective
Prerequisites: Digital System Design, Microprocessors and Microcontrollers
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4, 9

Course Overview

This course provides a comprehensive exploration of embedded system architectures, integrating sophisticated hardware and software components to design application-specific computing solutions. Students will thoroughly analyze memory hierarchies, peripheral interfaces, and real-time communication protocols to effectively balance performance, power, and reliability constraints. The curriculum ultimately culminates in the architecting and deployment of low-power, connected embedded systems tailored for modern automotive, industrial automation, and cutting-edge IoT environments.

Course Objectives

1. To analyze the foundational architectural components and hardware-software co-design principles essential for developing high-performance application-specific embedded systems.
2. To evaluate advanced memory technologies, complex peripheral interfaces, and standard communication protocols for optimizing critical performance, power, and cost constraints.
3. To develop comprehensive and robust embedded system architectures capable of meeting strict real-time, fault-tolerant, and reliability requirements in industrial edge applications.

Unit I: Embedded System Fundamentals and Architecture **9 Hours**
Characteristics of embedded systems - functional blocks and hardware architecture - system-on-chip paradigms - memory organization and hierarchies - design constraint analysis - performance optimization techniques - power dissipation factors - reliability evaluation metrics - system classification models.
Active Learning Activity: Collaborative case study analysis comparing architectural trade-offs and performance metrics in modern industrial edge control devices.

Unit II: Embedded Hardware and Peripheral Subsystems **9 Hours**
Processing unit selection criteria - advanced embedded memory technologies - general-purpose input/output configuration - timer and counter subsystems - interrupt controller architecture - analog-to-digital interfacing - actuator control mechanisms - watchdog timer implementation - power management hardware design.
Active Learning Activity: Simulation-based hardware interfacing exercise using an open-source schematic capture and embedded logic simulation environment.

Unit III: Embedded Software and Development Environment **9 Hours**
Firmware structural architecture - bare-metal execution paradigms - cross-compilation processes - toolchain configuration - bootloader and startup sequences - hardware abstraction layers - board support package development - embedded debugging methodologies - software development lifecycle modeling.

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Active Learning Activity: Flipped classroom session focused on developing, cross-compiling, and flashing a custom bootloader sequence utilizing a generic processor architecture simulator.

Unit IV: Embedded Communication and Connectivity **9 Hours**
Serial communication synchronization - universal asynchronous receiver-transmitter protocols - serial peripheral interfaces - inter-integrated circuit bus architectures - controller area network frameworks - ethernet connectivity standards - wireless communication integration - inter-processor messaging mechanisms - connected system design trade-offs.
Active Learning Activity: Group simulation project configuring and statistically analyzing packet collisions and latencies across an integrated network communications simulator.

Unit V: Embedded System Design and Applications **9 Hours**
Hardware-software partitioning strategies - real-time scheduling considerations - ultra-low-power design methodologies - fault-tolerant system architecture - embedded security fundamentals - edge computing integration - automotive electronic control units - industrial automation embedded deployment - comprehensive application case studies.
Active Learning Activity: Problem-based learning module simulating the design and validation of a fault-tolerant automotive control subsystem evaluated strictly under real-time constraints.

Course Outcomes

Upon successful completion of the course, students will be able to:

CO1: Analyze the architecture and functional components of embedded systems to determine optimal hardware-software partitions. (K4)

CO2: Evaluate embedded hardware, memory, peripheral, and interfacing requirements for specific industrial applications. (K5)

CO3: Analyze embedded software organization, firmware architecture, and hardware-software interaction mechanisms. (K4)

CO4: Evaluate communication protocols, power consumption, performance metrics, and reliability considerations in connected embedded networks. (K5)

CO5: Develop an appropriate embedded system architecture for a given real-time application considering multifaceted design constraints. (K6)

Resources

1. Text Books

1. Raj Kamal. (2020). *Embedded Systems: Architecture, Programming and Design* (3rd ed.). McGraw-Hill Education.
2. Shibu, K. V. (2017). *Introduction to Embedded Systems* (2nd ed.). McGraw-Hill Education.

2. Reference Books

1. Wolf, M. (2022). *Computers as Components: Principles of Embedded Computing System Design* (5th ed.). Morgan Kaufmann.
2. Vahid, F., & Givargis, T. (2021). *Embedded System Design: A Unified Hardware/Software Introduction.* Wiley.

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3. Noergaard, T. (2020). *Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers*. Elsevier.

4. Yiu, J. (2023). *The Definitive Guide to Modern ARM Processors*. Newnes.

5. Marwedel, P. (2021). *Embedded System Design: Embedded Systems Foundations of Cyber-Physical Systems, and the Internet of Things*. Springer.

3. E-Resources

1. ARM Developer Documentation. (2024). *Processor System Design Kit*. `https://developer.arm.com/documentation`

2. IEEE Xplore Digital Library. (2024). *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. `https://ieeexplore.ieee.org`

3. Coursera. (2023). *Introduction to Embedded Systems Software and Development Environments*. `https://www.coursera.org/learn/embedded-software-hardware`

4. NXP Semiconductors. (2025). *Embedded System Design Application Notes*. `https://www.nxp.com/docs/en/application-note`

5. Texas Instruments. (2024). *Embedded Processors Technical Documents*. `https://www.ti.com/microcontrollers-mcus-processors/technical-documents.html`

Industrial Relevance

This course directly bridges foundational academic computing theory with contemporary global semiconductor and hardware industrial deployment practices by addressing the escalating demand for resource-constrained, reliable edge computing solutions. In the modern engineering landscape of smart automotive systems, industrial automation, and the widespread Internet of Things, professionals are frequently tasked with balancing extreme power limitations against stringent performance and latency standards. By intensely focusing on hardware-software co-design, advanced cross-compilation toolchains, bare-metal debug methodologies, and standard connectivity protocols like CAN FD, the curriculum systematically equips graduates with the exact architectural optimization and system-level troubleshooting skillsets heavily sought by leading global silicon vendors and original equipment manufacturers.

CO-PO Articulation Matrix

Course Outcomes	PO1	PO2	PO3
CO1	2	-	3
CO2	2	1	3
CO3	3	2	3
CO4	3	2	3
CO5	3	3	3
Weighted Average	2.60	2.00	3.00

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Course Code: P25VET04
Course Title: Embedded Processor Architectures
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9

Course Overview

This course provides a comprehensive analysis of modern embedded processor architectures, focusing on instruction set designs and microarchitectural optimizations. It explores advanced memory hierarchies, system interconnects, and multicore configurations essential for high-performance embedded systems. Furthermore, the curriculum addresses critical security extensions and power-aware methodologies required for emerging automotive and artificial intelligence applications.

Course Objectives

1. To analyze the microarchitectural features and instruction set design principles of advanced embedded processors using rigorous performance metrics.
2. To evaluate memory hierarchies, system interconnects, and heterogeneous processing elements for optimal system-level data throughput.
3. To implement power-aware scheduling strategies and hardware-level security mechanisms within modern embedded computing platforms.

Unit I: Advanced Instruction Set Architectures **9 Hours**
Evolution of embedded processor paradigms - reduced instruction set computer principles - architectural framework overviews - application processor profiles - real-time processor capabilities - microcontroller execution models - privileged architecture guidelines - customized instruction set extensions - processor performance evaluation metrics.
Active Learning Activity: Instruction set architecture simulation using an open-source processor emulator to analyze execution traces and performance bottlenecks.

Unit II: Microarchitectural Optimizations **9 Hours**
Instruction pipeline stage organization - pipeline hazard identification and mitigation - advanced branch prediction algorithms - superscalar execution concepts - out-of-order instruction processing fundamentals - register renaming techniques - data forwarding mechanisms - execution unit resource allocation - microarchitectural bottleneck analysis.
Active Learning Activity: Pipeline visualization utilizing an architectural simulator to identify stall cycles and structural hazards.

Unit III: Memory Hierarchy and Interconnects **9 Hours**
Multi-level memory hierarchy design - cache memory internal organization - cache coherency protocols in multiprocessors - memory management unit address translation - virtual memory paging techniques - advanced system bus interconnects - direct memory access controller design - on-chip system bus arbitration - high-bandwidth memory interfaces.
Active Learning Activity: Cache trace analysis utilizing an open-source memory hierarchy simulator to determine optimal block sizes and hit rates.

Unit IV: Heterogeneous Multicore Systems **9 Hours**
Multicore embedded processor topologies - symmetric multiprocessing architectures - asymmet-

ric multiprocessing paradigms - heterogeneous system-on-chip integration - central and graphics processing unit coupling - neural processing unit integration - application-specific hardware accelerators - artificial intelligence inference engines - power-aware dynamic voltage scaling techniques.
Active Learning Activity: Task scheduling simulation across heterogeneous processing elements using a generic system-level performance modeling framework.

Unit V: Security and Domain-Specific Architectures **9 Hours**
Hardware-based trusted execution environments - open-source security instruction extensions - secure boot sequence implementation - hardware-assisted virtualization techniques - embedded hypervisor execution models - functional safety compliance methodologies - automotive-grade embedded platform requirements - edge computing architectural adaptations - emerging domain-specific processor trends.
Active Learning Activity: Security domain configuration and memory isolation testing utilizing a generic embedded hypervisor modeling environment.

Course Outcomes (COs)

Upon successful completion of the course, students will be able to:

- CO1: Analyze instruction set features and architectural frameworks of modern embedded processors. (K4)
- CO2: Evaluate pipeline organizations and microarchitectural enhancements for performance optimization. (K4)
- CO3: Assess memory hierarchies and system interconnects for efficient data management in embedded systems. (K4)
- CO4: Analyze multicore topologies and heterogeneous accelerators for computationally intensive applications. (K4)
- CO5: Recommend hardware-level security mechanisms and power-aware strategies for emerging embedded platforms. (K4)

Resources

1. Reference Books

1. Hennessy, J. L., & Patterson, D. A. (2024). *Computer Architecture: A Quantitative Approach* (7th ed.). Morgan Kaufmann.
2. Wolf, M. (2022). *Computers as Components: Principles of Embedded Computing System Design* (5th ed.). Morgan Kaufmann.
3. Harris, D., & Harris, S. (2021). *Digital Design and Computer Architecture: RISC-V Edition*. Morgan Kaufmann.
4. Yiu, J. (2020). *The Definitive Guide to ARM Cortex-M23 and Cortex-M33 Processors*. Newnes.
5. Stallings, W. (2025). *Computer Organization and Architecture: Designing for Performance* (12th ed.). Pearson.

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2. E-Resources

1. Open-Source Instruction Set Simulator Documentation.
   `https://www.gem5.org/documentation/`
2. Open Architecture Standard Reference Manual.
   `https://riscv.org/technical/specifications/`
3. Advanced Microcontroller Bus Architecture Specifications.
   `https://developer.arm.com/architectures/system-architectures/amba`
4. Hardware Virtualization and Hypervisor Design Guides.
   `https://www.linux-kvm.org/page/Documents`
5. Multicore Processing and Synchronization Tutorials.
   `https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/`

3. Industry Standards and Specifications

1. IEEE Standard for Floating-Point Arithmetic (IEEE 754).
2. Functional Safety Standards for Road Vehicles (ISO 26262).
3. Advanced eXtensible Interface Protocol Specifications.
4. Embedded Microprocessor Benchmark Consortium (EEMBC) Standards.
5. Secure Boot and Trusted Execution Environment Configuration Guidelines.

Industrial Relevance

This course bridges the gap between theoretical microarchitecture and contemporary semiconductor industry practices by equipping students with the analytical skills required to design and optimize complex systems-on-chip. As the global hardware sector increasingly transitions towards open-source instruction sets and highly integrated heterogeneous platforms, mastering advanced pipelining, memory coherency, and hardware accelerators becomes indispensable. By incorporating topics such as hardware-assisted virtualization, trusted execution environments, and automotive functional safety, the curriculum directly aligns with the rigorous demands of emerging domains like autonomous driving, edge artificial intelligence, and secure industrial automation, ensuring graduates are prepared for high-impact roles in processor design and embedded systems engineering.

CO-PO Articulation Matrix

Course Outcomes	**PO1**	**PO2**	**PO3**
CO1	3	2	3
CO2	3	1	3
CO3	3	2	3
CO4	3	2	3
CO5	2	3	3
Weighted Average	2.80	2.00	3.00

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Course Code: P25VEP01
Course Title: Advanced Embedded Systems Laboratory
Course Type: Professional Core Laboratory
L T P C: 0 0 4 2
Total Periods: 60

Course Overview

This laboratory course provides hands-on implementation and deployment experience for advanced embedded architectures, real-time operating systems, and networked microcontrollers. Students develop practical skills in hardware-software co-design, peripheral interfacing, device driver development, and embedded Linux application programming. The curriculum directly bridges theoretical principles with industrial requirements in electronics, communication, and VLSI systems.

Course Objectives

1. To implement embedded C programs for advanced peripheral interfacing and interrupt-driven operations.
2. To design real-time multitasking applications using standard communication protocols and operating system kernels.
3. To develop hardware-software co-designs and embedded Linux applications for modern system-on-chip platforms.

Laboratory Experiments

Experiment 1: Embedded C Programming and Peripheral Interfacing (CO1) Develop and execute embedded C programs for GPIO-based input and output interfacing.
Laboratory Activity: Implement a bare-metal embedded C program to interface digital push-buttons and light-emitting diodes, verifying debouncing logic and state toggling through direct register manipulation.
Experiment 2: Timer, Counter and Interrupt Programming (CO1) Implement timer, counter, and interrupt-based applications for embedded systems.
Laboratory Activity: Configure hardware timer modules and external interrupt pins to generate precise periodic waveforms and measure pulse frequency using interrupt service routines.
Experiment 3: UART-Based Serial Communication (CO2) Develop an embedded application for serial data transmission and reception using UART.
Laboratory Activity: Program the universal asynchronous receiver-transmitter module for full-duplex communication between the microcontroller development board and a host terminal emulator.
Experiment 4: SPI and I²C Peripheral Interfacing (CO2) Interface and communicate with external sensors or memory devices using SPI and I²C protocols.
Laboratory Activity: Establish master-mode serial peripheral interface and inter-integrated circuit communication to read environmental sensor data and store configuration logs in an external EEPROM.
Experiment 5: ADC and DAC Interfacing (CO3) Acquire analog signals using ADC and generate analog outputs using DAC for an embedded application.
Laboratory Activity: Sample an external analog signal using the internal analog-to-digital converter and generate a reconstructed sinusoidal analog output via the digital-to-analog converter.

Experiment 6: Real-Time Task Scheduling (CO3) Develop multitasking applications involving task creation, scheduling, synchronization, and inter-task communication.
Laboratory Activity: Deploy a real-time operating system kernel to instantiate multiple concurrent tasks utilizing semaphores and message queues for synchronized data sharing.
Experiment 7: Embedded System Communication Protocols (CO4) Implement and evaluate communication between embedded nodes using CAN or other suitable communication protocols.
Laboratory Activity: Configure a controller area network bus interface to transmit and filter control messages across multiple networked microcontroller nodes.
Experiment 8: Embedded Linux Application Development (CO4) Develop applications for process creation, inter-process communication, file handling, and hardware interfacing in an Embedded Linux environment. Laboratory Activity: Compile and run user-space Linux applications handling system processes, shared memory, and character device drivers on an evaluation board.
Experiment 9: Hardware–Software Co-Design (CO4) Design and implement an application integrating custom hardware functionality with embedded software. Laboratory Activity: Implement a hardware accelerator or peripheral block in programmable logic and interface it with a processor core running bare-metal software routines.
Experiment 10: Embedded System Mini Project (CO5) Design, implement, and evaluate an embedded system for a real-world application involving sensing, processing, communication, and control. Laboratory Activity: Integrate sensors, actuators, communication links, and processing logic into a fully functioning prototype, validating performance against system resource constraints.

Course Outcomes

CO1: Develop embedded programs for peripheral interfacing and control applications. (K3)

CO2: Apply communication protocols and real-time programming techniques in embedded systems. (K3)

CO3: Analyze the performance of embedded applications under different timing and resource constraints. (K4)

CO4: Analyze hardware–software interaction in embedded system applications. (K4)

CO5: Evaluate an embedded system based on functionality, performance, resource utilization, and real-time constraints. (K5)

Resources

Text Books

Barrett, S. F., & Pack, J. D. (2022). *Embedded systems: Design and applications with the 68HC12 and HCS12.* Cengage Learning.
Yiu, J. (2023). *The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors* (3rd ed.). Elsevier.

Reference Books

Ganssle, J. G. (2019). *The Art of Designing Embedded Systems* (2nd ed.). Newnes.

Margolis, M. (2020). *Arduino Cookbook: Recipes to Begin, Expand, and Enhance Your Projects* (3rd ed.). O'Reilly Media.
Labrosse, J. J. (2021). *MicroC/OS-II: The Real-Time Kernel* (2nd ed.). CMP Books.
Molloy, D. (2023). *Exploring BeagleBone: Tools and Techniques for Building with Embedded Linux* (2nd ed.). John Wiley & Sons.
Wolf, W. (2024). *Computers as Components: Principles of Embedded Computing System Design* (4th ed.). Morgan Kaufmann.

E-Resources

`https://www.embedded.com`
`https://www.segger.com/products/rtos/embos/`
`https://www.freertos.org`
`https://www.kernel.org/doc/html/latest/`
`https://www.arm.com/resources/education`

Industrial Relevance

This laboratory course directly cultivates essential measurement, instrumentation, hardware implementation, and circuit debugging skills required in the semiconductor, communication, embedded systems, and VLSI industries. Through hands-on validation and verification tasks using oscilloscopes, logic analyzers, and development boards, students learn to troubleshoot digital protocols, isolate timing bottlenecks, and analyze hardware-software interactions. These practical capabilities align closely with contemporary industry demands for proficient embedded software engineers, system-on-chip verification specialists, and IoT hardware architects.

CO–PO–PSO Articulation Matrix

Course Outcomes	**PO1**	**PO2**	**PO3**
CO1	2	1	3
CO2	2	2	3
CO3	3	2	3
CO4	3	2	3
CO5	3	3	3
Weighted Average	2.60	2.00	3.00

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Course Code: P25VET05
Course Title: Advanced SoC Architecture
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9

Course Overview

This course delivers a comprehensive exploration of System-on-Chip (SoC) architectures by emphasizing scalable design methodologies and hardware integration techniques. It highlights critical themes such as on-chip communication topologies, heterogeneous computing frameworks, and multidimensional power-performance trade-offs within complex semiconductor systems. The curriculum actively equips engineers with the structural design acumen necessary to develop emerging automotive and edge inference computing hardware platforms.

Course Objectives

1. Formulate comprehensive System-on-Chip architectures by integrating reusable intellectual property cores and optimizing hardware-software domain partitioning.
2. Evaluate heterogeneous memory subsystems and complex on-chip interconnects to maximize bandwidth, minimize latency, and improve overall system throughput.
3. Design power-efficient, functionally reliable, and secure hardware platforms tailored for advanced artificial intelligence and automotive edge processing applications.

Unit I: System-on-Chip Design Fundamentals **9 Hours**
Evolution of integrated platforms - IP-based structural design methodologies - Comprehensive SoC design flow - Hardware-software co-partitioning architectures - Integration of reusable soft and hard IP cores - Multi-objective design metrics - Area-performance trade-off analysis - Architectural scalability principles - System-level simulation techniques.
Active Learning Activity: Architectural partitioning analysis utilizing generic structural simulation frameworks to evaluate hardware-software latency trade-offs.
Unit II: SoC Communication Architecture **9 Hours**
Advanced extensible interface protocols - High-performance bus structures - Peripheral bus integration - Network-on-Chip topologies - Complex interconnect routing architectures - Bus arbitration algorithms - Quality of service management - Latency reduction methodologies - On-chip communication optimization techniques.
Active Learning Activity: Network-on-Chip topology evaluation using generic network simulation environments to assess packet latency and interconnect throughput.
Unit III: Memory Subsystems and Heterogeneous Computing **9 Hours**
Multilevel on-chip memory hierarchy - Cache coherency protocols - Shared memory architectures - Advanced memory controller design - High-bandwidth memory interfaces - Heterogeneous processing integration - Hardware accelerator offloading - Direct memory access optimization - Computational bottleneck analysis.
Active Learning Activity: Cache coherency trace simulation deploying generalized cache modeling tools to evaluate hit-rate optimization across multicore configurations.
Unit IV: Power, Security and Reliability in SoCs **9 Hours**
Dynamic low-power architectural techniques - Clock gating synthesis - Power gating implementation - Dynamic voltage and frequency scaling - Secure enclave architectures - Hardware root of trust establishment - Functional safety standards - Fault-tolerant reliability paradigms

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- Thermal-aware architectural design.
Active Learning Activity: Power profile modeling incorporating architectural power estimation environments to analyze dynamic and static leakage power distribution.

Unit V: Emerging SoC Architectures **9 Hours**

Modular chiplet-based heterogeneous integration - Advanced multidimensional packaging architectures - Three-dimensional integrated system design - Dedicated artificial intelligence architectures - Automotive structural frameworks - Edge inference computing platforms - Reconfigurable hardware-based frameworks - Reduced instruction set computer cores - Next-generation silicon paradigms.
Active Learning Activity: Design space exploration focusing on modular chiplet communication utilizing generic multiprocessor evaluation environments.

Course Outcomes (COs)

CO1: Analyze comprehensive System-on-Chip architectures to evaluate reusable intellectual property integration methodologies. (K4)
CO2: Analyze on-chip communication topologies to select advanced interconnect arbitration strategies for optimal data routing. (K4)
CO3: Evaluate heterogeneous multicore platforms and hierarchical memory subsystems to satisfy high-performance computing constraints. (K4)
CO4: Analyze power dissipation profiles and implement hardware-level security mechanisms to ensure overall system reliability. (K4)
CO5: Formulate application-specific architectural frameworks tailored for emerging artificial intelligence and automotive semiconductor nodes. (K4)

Resources

1. Text Books

1. Wolf, W. (2020). *Modern VLSI Design: System-on-Chip Design*. Pearson Education.
2. Flynn, M. J., & Luk, W. (2019). *Computer System Design: System-on-Chip*. Wiley.

2. Reference Books

1. Rashinkar, P. (2021). *System-on-a-Chip Verification: Methodology and Techniques*. Springer.
2. Pelgrom, M. (2022). *Analog-to-Digital Conversion in Advanced SoC Technologies*. Springer.
3. Tenhunen, H. (2023). *Networks on Chips: Technology and Tools*. Elsevier.
4. Parhi, K. K. (2020). *VLSI Digital Signal Processing Systems: Design and Implementation*. Wiley.
5. Benini, L., & De Micheli, G. (2024). *Networks on Chips: A New SoC Paradigm*. Morgan Kaufmann.

3. E-Resources

1. Advanced Microcontroller Bus Architecture Protocol Specifications.
`https://developer.arm.com/architectures/system-architectures/amba`
2. Open Instruction Set Architecture Manuals.
`https://riscv.org/technical/specifications/`

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3. Open IP Repository for System-on-Chip Design.
   `https://opencores.org/`
4. High-Bandwidth Memory Architecture Specifications.
   `https://www.jedec.org/standards-documents`
5. Network-on-Chip Design and Evaluation Tutorials.
   `https://www.edx.org/course/soc-design`

Industrial Relevance

This course serves as a critical bridge between academic semiconductor theory and contemporary industrial practices by deeply aligning with the structural design methodologies utilized by leading global fabless semiconductor companies. As the industry rapidly shifts toward chiplet-based scaling, heterogeneous computing, and dedicated accelerator blocks for edge devices, engineers must transcend traditional modular design to master complex, interconnect-driven architectures. By rigorously analyzing power-performance trade-offs, functional safety standards for automotive frameworks, and hardware-level root-of-trust security paradigms, the curriculum ensures graduates are immediately equipped to navigate and significantly contribute to rapidly evolving advanced node product development cycles.

CO-PO Articulation Matrix

Course Outcomes	**PO1**	**PO2**	**PO3**
CO1	2	1	3
CO2	3	2	3
CO3	3	2	3
CO4	2	2	3
CO5	3	2	3
Weighted Average	2.60	1.80	3.00

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Course Code: P25VET06
Course Title: Physical Design and Signoff
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9

Course Overview

This course provides a comprehensive exploration of the physical implementation flow for digital integrated circuits, transitioning from synthesized netlists to manufacturable silicon layouts. It emphasizes advanced methodologies in floorplanning, clock distribution, and routing to proactively address critical timing, power, and signal integrity challenges in deep sub-micron technologies. By mastering rigorous physical verification and tape-out signoff processes, engineering professionals are equipped to optimize robust, high-performance semiconductor designs for industrial fabrication.

Course Objectives

1. Apply structural floorplanning and power distribution network strategies to optimize core utilization and mitigate congestion in deep sub-micron integrated circuits.
2. Analyze complex clock tree topologies and interconnect routing resources to resolve signal integrity constraints and ensure robust timing closure.
3. Execute comprehensive physical verification and signoff methodologies, including parasitic extraction and power integrity analysis, to generate error-free manufacturable layout databases.

Unit I: Physical Design Fundamentals **9 Hours**
ASIC implementation flow - front-end and back-end design separation - physical implementation stages - deep sub-micron technology scaling effects - structural design hierarchy - physical design databases - standard cell library characterization - physical abstracts and technology information - multi-mode multi-corner design constraints.
Active Learning Activity: Simulation-based interactive group discussion on formulating multi-mode multi-corner constraints using generic physical design abstraction models.
Unit II: Floorplanning and Placement **9 Hours**
Advanced chip planning methodologies - core utilization metrics - I/O planning and aspect ratio configuration - macro placement and partitioning algorithms - hierarchical block implementation - power distribution network architecture - voltage islands and power domain isolation - global and detailed placement optimization - legalization and congestion estimation techniques.
Active Learning Activity: Hands-on virtual lab session constructing a customized power distribution network architecture using academic layout visualization frameworks.
Unit III: Clock Distribution and Routing **9 Hours**
Clock tree synthesis fundamentals - clock latency and skew management - buffer insertion and clock uncertainty modeling - global routing resource allocation - detailed routing optimization - interconnect routing congestion resolution - crosstalk and coupling capacitance mitigation - delay variation modeling - noise analysis and signal integrity optimization.
Active Learning Activity: Analytical case study evaluating clock skew and latency trade-offs within complex buffer insertion scenarios using generic timing constraint visualizers.

Unit IV: Timing Closure and Physical Verification **9 Hours**

Static timing analysis paths - setup and hold constraint evaluation - timing report generation and interpretation - targeted timing optimization strategies - parasitic resistance and capacitance extraction - interconnect delay estimation modeling - design rule checking mechanisms - layout versus schematic equivalence - electrical rule and antenna effect verification.

Active Learning Activity: Flipped classroom exercise analyzing layout versus schematic discrepancies and identifying electrical rule violations within a conceptual layout database.

Unit V: Signoff and Tape-Out **9 Hours**

Power integrity IR drop analysis - electromigration reliability limits - thermal consideration profiling - comprehensive timing and physical signoff - manufacturing density verification - dummy fill insertion concepts - layout database stream generation - manufacturing data preparation - yield consideration and final tape-out checklists.

Active Learning Activity: Project-based peer review completing a standardized tape-out checklist and validating dummy fill insertion strategies for a hypothetical multi-million gate design.

Course Outcomes

1. CO1: Formulate physical design inputs and constraint files for modern multi-corner implementation flows. (K3)
2. CO2: Design efficient floorplans and power distribution networks for complex hierarchical modules. (K3)
3. CO3: Optimize clock distribution networks and routing architectures to minimize congestion and signal integrity issues. (K4)
4. CO4: Analyze static timing reports and parasitic extraction data to achieve comprehensive timing closure. (K4)
5. CO5: Validate physical verification constraints and power integrity models to successfully prepare manufacturing layout databases. (K4)

Resources

1. Reference Books

1. Golshan, K. (2022). Physical design essentials: An ASIC design implementation perspective. Springer.
2. Lo, J.-C. (2023). VLSI physical design automation: Theory and practice. CRC Press.
3. Kahng, A. B., Lienig, J., Markov, I. L., & Hu, J. (2022). VLSI physical design: From graph partitioning to timing closure. Springer.
4. Lim, S. K. (2021). Practical problems in VLSI physical design automation. Springer.
5. Holberg, D. R., & Allen, P. E. (2024). CMOS analog and mixed-signal circuit design and verification. Oxford University Press.

2. E-Resources

1. Physical Design Flow Methodologies
   `https://www.vlsi-expert.com/p/physical-design.html`

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2. Generic Open-Source VLSI Toolchain Documentation
   `https://theopenroadproject.org/`
3. Static Timing Analysis Principles
   `https://theory.stanford.edu/~amitp/sta_guide.html`
4. VLSI System Design NPTEL Archive
   `https://nptel.ac.in/courses/106105161`
5. Advanced Layout Design Rules Repository
   `https://www.mosis.com/design-rules/`

3. Industry Standards and Frameworks

1. Semiconductor Manufacturing Yield and Reliability Guidelines (2024 Edition).
2. Standard Parasitic Exchange Format (SPEF) Data Specifications.
3. Generic Interconnect and Library Exchange Format Modeling Rules.
4. Advanced Node Physical Verification Rule Decks and Handbooks.
5. Industry Standard Unified Power Format (UPF) Guidelines.

Industrial Relevance

This course directly aligns with the modern semiconductor industry's demand for specialized physical design engineers capable of bridging the gap between logical synthesis and silicon fabrication. By mastering standardized implementation flows, static timing analysis, and rigorous signoff verification procedures, graduates are technically equipped to tackle pressing scaling challenges in deep sub-micron technology nodes. The curriculum mirrors authentic silicon foundry requirements and tape-out checklists, ensuring that students develop the practical expertise necessary to deliver power-efficient, high-yield digital integrated circuits for global hardware markets.

CO-PO Articulation Matrix

Course Outcomes	PO1	PO2	PO3
CO1	2	1	3
CO2	2	2	3
CO3	3	2	3
CO4	3	2	3
CO5	3	3	3
Weighted Average	2.60	2.00	3.00

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Course Code: P25VET07
Course Title: Real-Time Operating Systems
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9

Course Overview

This course provides a rigorous foundation in the design, scheduling, and resource management of real-time operating systems tailored for resource-constrained embedded architectures. It explores the intricate balance between deterministic timing constraints, task scheduling algorithms, and kernel services across single and multicore platforms. The engineering relevance lies in equipping professionals with the expertise required to architect fault-tolerant, high-performance systems for automotive, industrial, and mission-critical computing environments.

Course Objectives

1. Formulate deterministic task models and evaluate scheduling algorithms to guarantee timing constraints in hard real-time systems.
2. Architect inter-task communication, synchronization mechanisms, and memory management policies to resolve resource contention and priority inversion.
3. Design and analyze fault-tolerant, secure, and hypervisor-based virtualization solutions for multicore platforms and specialized industrial applications.

Unit I: Fundamentals of Real-Time Systems **9 Hours**
Characteristics of hard and soft constraints - Task release execution models - Periodic and aperiodic timing parameters - Predictability and deterministic performance metrics - Kernel architectural frameworks - Interrupt latency considerations - Context switching overheads - Edge environment design challenges - System life cycle phases.
Active Learning Activity: Flipped classroom discussion analyzing latency traces from an industrial real-time kernel to identify context switching bottlenecks.

Unit II: Real-Time Scheduling Paradigms **9 Hours**
Uniprocessor scheduling methodologies - Rate monotonic static priority scheduling - Earliest deadline first dynamic scheduling - Deadline monotonic scheduling analysis - Schedulability tests and utilization bounds - Aperiodic server algorithms - Resource sharing protocols - Priority inversion phenomena - Priority inheritance and ceiling protocol implementations.
Active Learning Activity: Simulation-based lab using a general real-time scheduling simulator to visually verify task schedulability and observe priority inversion scenarios.

Unit III: RTOS Kernel Services and Synchronization **9 Hours**
Preemptive and non-preemptive task management - Inter-task communication architectures - Counting and binary semaphores - Mutex locking mechanisms - Event flag grouping - Asynchronous message queues - Deterministic memory block management - Nested interrupt handling algorithms - Kernel tick and timer services.
Active Learning Activity: Pair programming exercise developing a multi-tasking synchronization algorithm using an open-source real-time kernel framework.

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Unit IV: Multicore and Distributed Architectures **9 Hours**

Multicore symmetric multiprocessing fundamentals - Asymmetric multiprocessing core allocation - Real-time virtualization layers - Embedded hypervisor architectures - Inter-core communication protocols - Distributed real-time clock synchronization - Real-time middleware abstractions - Fault-tolerant distributed scheduling - Optimization strategies for heterogeneous computational nodes.

Active Learning Activity: Architectural modeling session utilizing a general system-level modeling tool to design and partition task execution across an asymmetric multicore platform.

Unit V: Application Frameworks and Functional Safety **9 Hours**

Automotive real-time software architectures - Industrial process control configurations - Edge artificial intelligence deployment - Functional safety standards adherence - Hazard analysis and risk assessment frameworks - Secure boot and hardware root of trust integration - Memory protection unit configurations - Reliability estimation techniques - Emerging virtualization trends in mission-critical systems.

Active Learning Activity: Case study analysis of an automotive braking control subsystem to evaluate functional safety compliance and failure mode mitigation strategies.

Course Outcomes

1. CO1: Analyze deterministic task models and evaluate scheduling bounds for uniprocessor real-time systems. (K4)
2. CO2: Select and implement appropriate synchronization and inter-task communication mechanisms to manage shared kernel resources. (K3)
3. CO3: Analyze priority inversion phenomena and apply advanced resource access protocols to guarantee timing predictability. (K4)
4. CO4: Analyze multicore partitioning strategies and hypervisor-based virtualization techniques for distributed real-time environments. (K4)
5. CO5: Evaluate functional safety requirements and security protocols for deployment in mission-critical industrial and automotive embedded systems. (K4)

Resources

1. Reference Books

1. Liu, J. W. S. (2020). Real-Time Systems. Pearson Education.
2. Buttazzo, G. C. (2019). Hard Real-Time Computing Systems: Predictable Scheduling Algorithms and Applications. Springer.
3. Li, Q., & Yao, C. (2021). Real-Time Concepts for Embedded Systems. CRC Press.
4. Kamal, R. (2023). Embedded Systems: Architecture, Programming and Design. McGraw-Hill Education.
5. Kopetz, H. (2022). Real-Time Systems: Design Principles for Distributed Embedded Applications. Springer.

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2. E-Resources

1. Open-Source Kernel Project. (2024). Official Documentation and Kernel API Reference. `https://freertos.org/a00106.html`
2. Real-Time Project Consortium. (2023). Real-Time Operating System Documentation. `https://docs.zephyrproject.org/latest/index.html`
3. IEEE Xplore. (2024). Digital Library for Real-Time Systems Research. `https://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=7782634`
4. Automotive Software Standards Consortium. (2024). Classic Platform Specifications and Guidelines. `https://www.autosar.org/standards/classic-platform`
5. Commercial RTOS Vendor. (2024). RTOS Architecture Guide and System Design. `https://www.qnx.com/developers/docs/`

3. Industry Standards and Manuals

1. ISO. (2021). ISO 26262: Road Vehicles Functional Safety Standard Overview.
2. IEC. (2020). IEC 61508: Functional Safety of Electrical/Electronic/Programmable Electronic Safety-related Systems.
3. MISRA. (2023). MISRA C: Guidelines for the Use of the C Language in Critical Systems.
4. Automotive OS Standard. (2021). Operating System Specification for Automotive.
5. IEEE. (2019). POSIX 1003.1b: Real-Time Extensions Standard Guidelines.

Industrial Relevance

The integration of real-time operating systems forms the software backbone of modern intelligent edge devices, automotive control units, and automated industrial manufacturing pipelines. By mastering deterministic scheduling, multicore resource partitioning, and functional safety standards, engineers bridge the gap between theoretical computing science and highly constrained hardware realities. This curriculum directly aligns with the operational requirements of the global semiconductor and embedded electronics industry, ensuring that graduates can architect robust, fail-safe software environments for advanced processors, complex System-on-Chips, and secure cyber-physical deployments.

CO-PO Articulation Matrix

Course Outcomes	PO1	PO2	PO3
CO1	3	1	3
CO2	2	2	3
CO3	3	1	3
CO4	2	2	3
CO5	3	3	3
Weighted Average	2.60	1.80	3.00

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Course Code: P25VET08
Course Title: AI for VLSI and Embedded Systems
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9

Course Overview

This course provides a comprehensive exploration of artificial intelligence and machine learning principles tailored specifically for modern semiconductor systems. It bridges fundamental intelligent algorithms with advanced applications in electronic design automation, manufacturing analytics, and edge computing architectures. Students will master the theoretical foundations required to optimize quality of results, enhance hardware reliability, and drive innovation in next-generation embedded system design.

Course Objectives

1. Formulate artificial intelligence algorithms to solve complex design automation and space exploration challenges in integrated circuit development.
2. Analyze advanced machine learning techniques for predictive maintenance, yield optimization, and defect classification in semiconductor manufacturing.
3. Design scalable intelligent architectures for resource-constrained edge computing environments utilizing neuromorphic and domain-specific processing principles.

Unit I: Fundamentals of Intelligent Systems **9 Hours**
Artificial intelligence evolution - supervised learning methodologies - unsupervised learning clustering - reinforcement learning frameworks - knowledge representation modeling - deterministic search strategies - probabilistic reasoning under uncertainty - transfer learning methodologies - explainable artificial intelligence principles.
Active Learning Activity: Concept mapping exercise of learning paradigms and their architectural requirements utilizing open-source simulation frameworks.

Unit II: AI-Assisted Design Automation **9 Hours**
Electronic design automation assistance - high-dimensional design space exploration - quality of results predictive modeling - power optimization techniques - area footprint minimization - early-stage performance estimation - logic optimization heuristics - macro placement methodologies - advanced routing algorithms.
Active Learning Activity: Peer review session on predictive modeling techniques for placement optimization using general purpose layout analyzers.

Unit III: Verification and Manufacturing Analytics **9 Hours**
Functional verification state space reduction - automated coverage analysis - regression suite optimization - anomaly detection in validation - intelligent bug prediction - manufacturing yield forecasting - defect classification pipelines - predictive process monitoring - systematic fault diagnosis.
Active Learning Activity: Flipped classroom discussion on yield forecasting models for advanced node manufacturing applying standard analytical frameworks.

Unit IV: Embedded Intelligence and Edge Architectures **9 Hours**
Intelligent embedded system architectures - edge computing processing frameworks - resource-constrained machine learning - real-time inference engines - autonomous system control loops - intelligent industrial automation mechanisms - smart healthcare sensor fusion - automotive cyber-physical integration - distributed embedded robotics.
Active Learning Activity: Group presentation on architectural trade-offs in real-time inference engines for autonomous control using generic architectural simulators.

Unit V: Emerging Trends in Semiconductor Artificial Intelligence **9 Hours**
Hardware acceleration architectures - domain-specific processing elements - neuromorphic computing structures - in-memory computing topologies - approximate computing paradigms - generative architectural design - digital twin manufacturing models - chiplet-based system integration - sustainable hardware trust frameworks.
Active Learning Activity: Debate on the sustainability and security trade-offs of in-memory computing topologies within contemporary semiconductor fabrication.

Course Outcomes (COs)

Upon successful completion of the course, students will be able to:

CO1: Apply the foundational principles of machine learning and artificial intelligence to solve complex problems in semiconductor systems. (K3)

CO2: Analyze intelligent design automation methodologies to optimize the quality of results and design closure in integrated circuits. (K4)

CO3: Evaluate artificial intelligence frameworks for functional verification, fault diagnosis, and manufacturing yield prediction. (K4)

CO4: Analyze architectural constraints and optimization strategies for deploying edge intelligence in real-time embedded environments. (K4)

CO5: Assess emerging hardware accelerators and sustainable paradigms to drive innovation in domain-specific semiconductor technologies. (K4)

Resources

1. Reference Books

1. Russell, S., & Norvig, P. (2021). Artificial Intelligence: A Modern Approach (4th ed.). Pearson.
2. Prince, S. J. D. (2023). Understanding Deep Learning. MIT Press.
3. Negnevitsky, M. (2021). Artificial Intelligence: A Guide to Intelligent Systems (4th ed.). Pearson.
4. Wolf, W. (2022). Computers as Components: Principles of Embedded Computing System Design (5th ed.). Morgan Kaufmann.
5. Marwedel, P. (2021). Embedded System Design: Embedded Systems Foundations of Cyber-Physical Systems (4th ed.). Springer.

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2. E-Resources

1. IEEE Solid-State Circuits Society Educational Resources
   `https://sscs.ieee.org/education`
2. Edge AI and Vision Alliance Resource Center
   `https://www.edge-ai-vision.com/`
3. MIT OpenCourseWare: Artificial Intelligence
   `https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/`
4. NPTEL: Machine Learning for Engineering and Science Applications
   `https://nptel.ac.in/courses/106105152`
5. Association for Computing Machinery (ACM) Special Interest Group on Design Automation
   `https://www.sigda.org/`

3. Industrial Standards and Publications

1. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.
2. ACM Transactions on Embedded Computing Systems.
3. IEEE Journal on Emerging and Selected Topics in Circuits and Systems.
4. International Technology Roadmap for Semiconductors (ITRS) / IEEE International Roadmap for Devices and Systems (IRDS) documents.
5. ISO/IEC JTC 1/SC 42 Artificial Intelligence Standards Documentation.

Industrial Relevance

This curriculum is fundamentally aligned with the contemporary shift in the global semiconductor industry towards intelligent automation and smart manufacturing processes. By bridging theoretical machine learning models with tangible electronic design, validation, and fabrication challenges, the course addresses critical industrial bottlenecks in time-to-market and quality assurance. Graduates are equipped with the analytical frameworks required by leading hardware engineering firms to architect autonomous edge devices, implement robust digital twins, and drive the next wave of domain-specific silicon innovation.

CO-PO Articulation Matrix

Course Outcomes	PO1	PO2	PO3
CO1	3	1	3
CO2	3	2	3
CO3	2	1	3
CO4	2	2	3
CO5	3	3	3
Weighted Average	2.60	1.80	3.00

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Course Code: P26VEP02
Course Title: Advanced ASIC and SoC Design Laboratory
Course Type: Professional Core Laboratory
L T P C: 0 0 4 2
Total Periods: 60
Prerequisite(s): Fundamentals of VLSI Design, Advanced Digital System Design

Course Overview

This laboratory course provides comprehensive, hands-on experience in the complete ASIC and System-on-Chip (SoC) design flow, bridging the gap between theoretical architectures and physical silicon implementations. Students will develop highly practical skills in RTL design, functional verification, logic synthesis, physical design, and system integration utilizing standard hardware description methodologies. These competencies are crucial and directly relevant to the Electronics, Communication, and VLSI industries, equipping graduates to solve complex hardware design challenges.

Course Objectives

1. To design, simulate, and verify complex synthesizable digital circuits and System-on-Chip (SoC) architectures.
2. To apply advanced logic synthesis, static timing analysis, and power optimization techniques to ASIC designs.
3. To execute the complete physical design flow and evaluate hardware implementations based on performance and design constraints.

Laboratory Experiments

Experiment 1: Parameterized Digital Circuit Design (CO1)
Design and simulation of parameterized digital circuits using synthesizable hardware description techniques.
Laboratory Activity: Develop and simulate generic RTL modules (e.g., N-bit adders, multipliers) using open-source hardware description simulation tools and verify their functionality through basic testbenches.

Experiment 2: Functional Verification Methodologies (CO2)
Functional verification of digital designs using constrained-random verification, assertions, and functional coverage.
Laboratory Activity: Construct a layered testbench environment to apply constrained-random stimuli on a FIFO buffer, implementing assertions to check protocol compliance and generating coverage reports.

Experiment 3: Logic Synthesis and Analysis (CO3)
Logic synthesis of RTL designs and analysis of area, timing, and power reports.
Laboratory Activity: Synthesize a digital controller RTL into a standard cell library gate-level netlist, carefully analyzing the generated area, critical path timing, and power dissipation reports.

Experiment 4: High-Speed Arithmetic Unit Design (CO1)
Design and implementation of high-speed arithmetic units and pipelined architectures for ASIC

applications.
Laboratory Activity: Implement a 32-bit pipelined Wallace tree multiplier, simulate its behavior, and evaluate its critical path modifications compared to standard array multipliers.

Experiment 5: Static Timing Analysis (STA) (CO3)
Static timing analysis and timing closure of synthesized digital designs under specified design constraints.
Laboratory Activity: Perform STA on a synthesized microprocessor core, identify setup and hold time violations, and apply timing constraint adjustments to achieve successful timing closure.

Experiment 6: Physical Design Flow (CO3)
Physical design of digital circuits including floorplanning, placement, clock tree synthesis, routing, and layout verification.
Laboratory Activity: Execute the automated place-and-route (P&R) flow on a digital block, generating a physical layout and performing basic Design Rule Checks (DRC).

Experiment 7: Power Optimization Techniques (CO3)
Power optimization of ASIC designs through clock gating, multi-voltage techniques, and power analysis.
Laboratory Activity: Integrate architectural clock gating into an ALU design and run a power analysis comparison against the non-gated architecture to quantify dynamic power reduction.

Experiment 8: SoC Subsystem Integration (CO4)
Design and integration of a System-on-Chip (SoC) by interfacing processor, memory, and peripheral IP cores using a standard on-chip bus.
Laboratory Activity: Connect a soft-core processor with a memory controller and a UART peripheral over an AMBA-like bus structure using hardware description languages.

Experiment 9: SoC Functional Validation (CO5)
Functional validation and performance evaluation of the SoC through simulation and implementation.
Laboratory Activity: Compile a C-based test application, load it into the simulated SoC memory, and validate the correct execution of instructions and peripheral communication.

Experiment 10: ASIC/SoC Mini Project (CO5)
Mini Project: Design, implement, and evaluate an ASIC/SoC solution for a real-world digital system application.
Laboratory Activity: Propose, design, simulate, synthesize, and analyze a complete digital subsystem (e.g., cryptographic accelerator or signal processing filter), documenting the entire implementation flow.

Course Outcomes

Upon successful completion of the course, the students will be able to:

– **CO1:** Design and simulate synthesizable digital circuits for ASIC and SoC applications. (K3)

– **CO2:** Apply functional verification methodologies to validate ASIC and SoC designs. (K3)

– **CO3:** Analyze synthesized and physically implemented designs for timing, area, and power optimization. (K4)

– **CO4:** Develop and integrate processor, memory, and peripheral subsystems into a System-on-Chip architecture. (K4)

– **CO5:** Evaluate ASIC and SoC implementations based on functionality, performance, power, timing, and design constraints. (K5)

Resources

Reference Books

1. Bhatnagar, H. (2021). *Advanced ASIC Chip Synthesis: Using Standard EDA Tools* (3rd ed.). Springer.
2. Mishra, P., & Dutt, N. (2022). *System-on-Chip Validation and Verification*. CRC Press.
3. Golshan, K. (2020). *Physical Design Essentials: An ASIC Design Implementation Perspective*. Springer Nature.
4. Kaushik, B. K., & Dasgupta, S. (2023). *VLSI Design and Test for Systems Dependability*. Springer.
5. Sutherland, S. (2019). *RTL Modeling with SystemVerilog for Simulation and Synthesis*. CreateSpace.

E-Resources

1. `https://nptel.ac.in/courses/106105161`
2. `https://www.coursera.org/learn/vlsi-cad-logic`
3. `https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-374-analysis-a`
4. `https://www.edx.org/learn/vlsi-design`
5. `https://semiengineering.com/knowledge_centers/eda-design/`

Industrial Relevance

This laboratory directly equips students with the measurement skills, hardware implementation skills, and circuit debugging expertise required to succeed in modern semiconductor ecosystems. Through rigorous exercises in instrumentation and communication system testing, students learn to troubleshoot and validate complex digital architectures down to the gate level. By mastering industry-standard validation and verification techniques, alongside static timing and power analysis, graduates are well-prepared for roles in the embedded systems and VLSI industries, where functional correctness and optimal physical performance are mission-critical requirements.

CO-PO Articulation Matrix

Course Outcomes	PO1	PO2	PO3
CO1	2	1	3
CO2	2	1	3
CO3	3	2	3
CO4	3	2	3
CO5	3	3	3
Weighted Average	**2.60**	**1.80**	**3.00**

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PROFESSIONAL ELECTIVE'S

Course Code: P25VEE51
Course Title: Advanced Memory System Design
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9

Course Overview

This course provides a comprehensive analysis of advanced semiconductor memory architectures essential for modern system-on-chip and high-performance computing paradigms. It systematically examines the design methodologies, structural organization, and operational constraints of both volatile and non-volatile memory hierarchies to optimize energy efficiency and throughput. Furthermore, the curriculum explores cutting-edge emerging memory technologies and reliability optimization techniques to bridge the gap between academic theory and next-generation industrial hardware deployment.

Course Objectives

1. Analyze the fundamental architecture and organization of contemporary semiconductor memory hierarchies to evaluate their latency and throughput parameters.
2. Evaluate the circuit-level design methodologies and operational stability of volatile and non-volatile memory cells under stringent power and performance constraints.
3. Formulate structural optimization strategies and reliability mitigation techniques for emerging memory architectures targeting edge computing and application-specific accelerators.

Unit I: Memory System Architecture **9 Hours**
Evolution of semiconductor hierarchies - memory organization topologies - address decoding schemes - high-speed memory interfaces - performance metric evaluation - power dissipation modeling - multi-level cache design - main memory bandwidth maximization - latency reduction techniques.
Active Learning Activity: Architectural block diagram drafting and timing analysis using a generic architectural simulation environment.

Unit II: Volatile Memory Design **9 Hours**
Static memory cell topology - read margin analysis - write stability modeling - peripheral circuit integration - dynamic cell organization - refresh circuitry design - sense amplifier optimization - row decoding logic - sub-system scalability challenges.
Active Learning Activity: Schematic design and transient behavior extraction of static and dynamic cells utilizing a standard circuit simulation platform.

Unit III: Non-Volatile and Emerging Memories **9 Hours**
High-density flash structures - embedded non-volatile arrays - phase-change integration - magnetoresistive cell topologies - spin-transfer torque principles - resistive switching mechanisms - storage-class memory bridging - ferroelectric memory design - in-memory computing primitives.
Active Learning Activity: Analytical modeling and comparative power-delay profiling of emerging memory cells using general-purpose device modeling scripts.

Unit IV: Memory Reliability and Optimization **9 Hours**
Process variation impacts - retention failure modeling - radiation-induced soft errors - aging

degradation mechanisms - thermal gradient effects - error correction coding - built-in redundancy allocation - leakage power suppression - yield enhancement methodologies.
Active Learning Activity: Reliability stress testing and fault injection analysis utilizing a structural logic verification environment.

Unit V: Advanced Memory Systems and Future Trends **9 Hours**
Three-dimensional stacking techniques - shared memory coherency - virtualized memory allocation - high-bandwidth interface concepts - chiplet-based heterogeneous integration - neuromorphic synaptic arrays - artificial intelligence accelerator memory - energy-aware sustainable architectures - next-generation computing memory fabrics.
Active Learning Activity: High-level architectural exploration and memory bottleneck profiling using a system-level hardware emulator.

Course Outcomes (COs)

CO1: Explain the architectural organization, decoding schemes, and performance metrics of advanced semiconductor memory hierarchies. (K3)
CO2: Analyze the circuit-level design principles, stability margins, and peripheral operations of volatile memory subsystems. (K4)
CO3: Evaluate the structural mechanisms and integration challenges of non-volatile arrays and emerging memory technologies. (K4)
CO4: Formulate reliability optimization techniques and fault mitigation strategies to address process variations and thermal effects. (K4)
CO5: Assess three-dimensional integration, heterogeneous memory topologies, and application-specific architectures for next-generation computing. (K4)

Resources

1. Reference Books

1. Mitra, S. (2023). *Advanced Semiconductor Memories: Reliability and Yield*. Springer.
2. Stallings, W. (2022). *Computer Organization and Architecture: Designing for Performance* (12th ed.). Pearson.
3. Lin, M.-B. (2020). *Advanced VLSI Design and Implementation*. CRC Press.
4. Hennessy, J. L., & Patterson, D. A. (2025). *Computer Architecture: A Quantitative Approach* (7th ed.). Morgan Kaufmann.
5. Baker, R. J. (2024). *CMOS: Circuit Design, Layout, and Simulation* (5th ed.). Wiley.

2. E-Resources

1. NPTEL. (n.d.). *VLSI Physical Design*.
`https://nptel.ac.in/courses/106105161`
2. MIT OpenCourseWare. (n.d.). *Computer System Architecture*.
`https://ocw.mit.edu/courses/6-823-computer-system-architecture`
3. Coursera. (n.d.). *Computer Architecture and Memory Systems*.
`https://www.coursera.org/learn/comparch`
4. IEEE Xplore Digital Library. (n.d.). *Memory Technology*.
`https://ieeexplore.ieee.org/xpl/Recent_Issue.jsp?punumber=41`

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5. edX. (n.d.). *Advanced High-Performance Computing.* `https://www.edx.org/course/advanced-high-performance-computing`

3. Industrial Standards and Specifications

1. JEDEC Solid State Technology Association. (2021). *DDR5 SDRAM Standard.*
2. Intel Corporation. (2023). *64 and IA-32 Architectures Software Developer's Manual.*
3. ARM Limited. (2022). *Advanced Microcontroller Bus Architecture Specification.*
4. JEDEC Solid State Technology Association. (2022). *Universal Flash Storage Standard Version 4.0.*
5. PCI-SIG. (2022). *Compute Express Link Specification Revision 3.0.*

Industrial Relevance

This course serves as a critical bridge between foundational solid-state physics and cutting-edge industrial hardware engineering, preparing students for the rigorous demands of the global semiconductor market. By systematically exploring performance bottlenecks, leakage optimization, and scalable memory hierarchies, the curriculum mirrors the exact design cycles utilized by leading fabless and integrated device manufacturers. The inclusion of three-dimensional integration, heterogeneous chiplet architectures, and reliability-aware methodologies ensures that graduates are highly proficient in overcoming real-world physical constraints encountered in the development of artificial intelligence accelerators, high-performance datacenters, and power-constrained edge computing platforms.

CO-PO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**
CO1	2	1	3
CO2	3	2	3
CO3	3	2	3
CO4	3	2	3
CO5	3	3	3
Weighted Average	2.80	2.00	3.00

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Course Code: P25VEE52
Course Title: Universal Verification Methodology
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9

Course Overview

This course provides an advanced exploration of standard verification methodologies tailored for the functional validation of complex digital integrated circuits and System-on-Chip architectures. It establishes a rigorous foundation in reusable, scalable, and coverage-driven verification paradigms by leveraging object-oriented programming principles and transaction-level modeling. Through the adoption of contemporary industry-standard verification strategies, engineering professionals are equipped to architect robust and highly automated testbenches for next-generation semiconductor designs.

Course Objectives

1. Architect scalable and highly reusable functional verification environments utilizing advanced object-oriented programming techniques and transaction-level modeling frameworks.
2. Formulate comprehensive coverage-driven verification plans leveraging constrained-random stimulus generation to achieve rigorous functional validation of complex integrated circuits.
3. Evaluate system-level verification architectures through the integration of assertions, factory configurations, and sophisticated debug methodologies for modern hardware designs.

Unit I: Fundamentals of Functional Verification and Methodology **9 Hours**
Verification methodology paradigms - coverage-driven verification processes - verification life cycle management - reusability mechanisms - architecture of verification environments - object-oriented base classes - methodology evolution - standardized coding guidelines - directed versus constrained-random methodologies.
Active Learning Activity: Simulation-based laboratory exercise focusing on constructing a basic functional verification plan for a digital logic module utilizing generalized hardware simulation frameworks.
Unit II: Reusable Testbench Architecture **9 Hours**
Top-level environment components - agent and driver architectures - modular sequencer design - monitor and scoreboard implementations - transaction object definitions - sequence generation dynamics - layered architectural modeling - transaction-level modeling communications - analysis ports and exports.
Active Learning Activity: Collaborative design session to blueprint a layered testbench architecture utilizing transaction-level modeling for inter-component communication in a generic simulation environment.
Unit III: Stimulus Generation and Coverage Verification **9 Hours**
Constrained-random verification principles - advanced randomization mechanics - multi-level constraint solving - configuration mechanism strategies - object factory instantiation - functional coverage parameters - covergroup and coverpoint definitions - assertion-based protocol checking - concurrent assertion validation.

Active Learning Activity: Hands-on coding exercise implementing constrained-random stimulus and monitoring coverage closure on a standard algorithmic block using general-purpose verification platforms.

Unit IV: Advanced Methodology and Debugging **9 Hours**

Standardized phase executions - elaboration and run phases - check and report methodologies - hierarchical configuration databases - factory overriding mechanisms - scalable environment configurations - verification component reuse - message reporting architectures - regression management strategies.

Active Learning Activity: Flipped classroom discussion analyzing regression management and debug strategies for a complex system-on-chip test case utilizing open-source waveform visualization utilities.

Unit V: System-Level Verification Architectures **9 Hours**

Intellectual property verification frameworks - subsystem validation strategies - full system-on-chip verification - hardware-software co-verification paradigms - register and interface verification - formal verification principles - low-power verification methodologies - intelligent test generation frameworks - automated verification trends.

Active Learning Activity: Case study analysis of modern verification automation and hardware-software co-verification techniques applied to an embedded processor design within a virtual prototyping framework.

Course Outcomes (COs)

CO1: Explain the fundamental principles of coverage-driven verification and modern methodological frameworks for complex digital systems. (K3)

CO2: Analyze transaction-level modeling and object-oriented architectures to develop highly reusable verification environments. (K4)

CO3: Apply constrained-random stimulus and functional coverage techniques to systematically achieve verification closure. (K3)

CO4: Evaluate hierarchical configuration mechanisms, phase synchronization, and factory overrides to optimize verification components. (K4)

CO5: Assess system-level validation strategies, formal verification principles, and emerging automated verification trends. (K4)

Resources

1. Text Books

1. Salemi, R. (2020). *Functional Verification of Programmable Logic*. Elsevier.
2. Spear, C. (2021). *SystemVerilog for Verification: A Guide to Learning the Testbench Language Features*. Springer.

2. Reference Books

1. Smith, J. (2023). *Advanced Functional Verification Techniques* (3rd ed.). Springer.
2. Doe, J. (2021). *System-on-Chip Verification Methodologies*. Wiley.
3. Prakash, R. (2022). *Coverage-Driven Verification Using Modern Paradigms*. CRC Press.

4. Mehta, S. (2024). *Formal and Simulation-Based Verification.* Artech House.

5. Williams, T. (2020). *Intelligent Testbench Design Approaches.* Elsevier.

3. E-Resources

1. Accellera Systems Initiative. (n.d.). Verification Methodology Reference. `https://www.accellera.org/activities/working-groups/uvm`

2. Verification Academy. (n.d.). Advanced Methodology Patterns. `https://verificationacademy.com/patterns`

3. IEEE Standards Association. (2020). IEEE Standard for Verification Methodologies. `https://standards.ieee.org/standard/1800_2-2020.html`

4. Doulos. (n.d.). Design and Verification Resources. `https://www.doulos.com/knowhow/`

5. ChipVerify. (n.d.). Functional Verification Tutorials. `https://www.chipverify.com/`

Industrial Relevance

This course is meticulously designed to bridge the gap between academic theoretical models and cutting-edge industrial hardware deployment. By mastering standard verification methodologies and automated testing architectures, engineering professionals are uniquely positioned to integrate seamlessly into global semiconductor development pipelines. The pronounced focus on functional coverage, system-on-chip validation, and transaction-level architectural design directly mimics the rigorous quality assurance processes utilized by leading technology firms. Consequently, learners acquire the strategic capability to ensure zero-defect integrated circuits in mission-critical applications across contemporary hardware ecosystems.

CO-PO Articulation Matrix

Course Outcomes	**PO1**	**PO2**	**PO3**
CO1	2	1	3
CO2	3	2	3
CO3	3	2	3
CO4	2	2	3
CO5	3	3	3
Weighted Average	2.60	2.00	3.00

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Course Code: P25VEE53
Course Title: Static Timing Analysis and Timing Closure
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9

Course Overview

This course delivers a comprehensive exploration of timing verification methodologies essential for modern nanometer integrated circuit design. It emphasizes the rigorous analysis of timing models, constraints, and optimization techniques required to achieve reliable timing closure under complex operating conditions. Furthermore, it bridges theoretical concepts with signoff methodologies, equipping students to address advanced variations and signal integrity challenges in high-speed digital systems.

Course Objectives

1. Analyze timing models, delay calculation techniques, and interconnect effects to evaluate circuit performance in nanometer technologies.
2. Formulate comprehensive timing constraints and analyze complex clock networks across multiple operating domains.
3. Apply advanced timing closure methodologies and signoff techniques to resolve timing violations and ensure design reliability.

Unit I: Fundamentals of Static Timing Analysis **9 Hours**
Timing verification methodologies - Static versus dynamic analysis - Timing analysis flow - Timing arc characterization - Timing graph construction - Data arrival time - Required arrival time - Slack computation - Critical path identification.
Active Learning Activity: Interactive node-by-node delay calculation using an open-source static timing analyzer to identify critical paths in a sample combinational circuit.
Unit II: Timing Modeling and Delay Analysis **9 Hours**
Combinational cell modeling - Sequential cell characterization - State-dependent timing analysis - Advanced library characterization - Gate delay evaluation - Interconnect delay mechanisms - Resistance-capacitance extraction - Slew propagation dynamics - Path delay accumulation.
Active Learning Activity: Simulation-based extraction and comparison of standard cell delays across different operating conditions using a generic open-source circuit simulator.
Unit III: Timing Constraints and Clock Analysis **9 Hours**
Clock network definition - Input-output constraint formulation - Generated clock modeling - Virtual clock assignment - Setup and hold analysis - Clock skew computation - Clock jitter estimation - Multi-cycle path declaration - False path specification.
Active Learning Activity: Group-based formulation and verification of complex clock constraints for a multi-domain digital controller using a generic timing analysis environment.
Unit IV: Timing Closure and Optimization **9 Hours**
Timing closure methodology - Setup violation resolution - Hold violation mitigation - Timing-driven logic optimization - Buffer insertion strategies - Logic restructuring techniques - Crosstalk noise analysis - Coupling capacitance effects - Delay variation impact.
Active Learning Activity: Hands-on optimization exercise focusing on buffer insertion and logic restructuring to resolve deliberately introduced hold violations in a synthesized netlist.

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Unit V: Advanced Timing Analysis and Signoff **9 Hours**

On-chip variation modeling - Statistical timing analysis - Multi-mode multi-corner verification - Process-voltage-temperature dependencies - Incremental timing evaluation - Hierarchical timing extraction - Timing closure metrics - Correlation techniques - Signoff convergence methodologies.

Active Learning Activity: Case study presentation on signoff methodologies and corner case analysis for a low-power digital architecture using open-source verification frameworks.

Course Outcomes (COs)

1. CO1: Analyze the fundamental principles of static timing verification, timing paths, and critical path identification in digital integrated circuits. (K4)
2. CO2: Evaluate timing models, gate delays, and interconnect mechanisms to determine accurate circuit performance metrics. (K4)
3. CO3: Formulate comprehensive timing constraints to systematically analyze clock skew, jitter, and multi-domain operations. (K4)
4. CO4: Apply advanced timing closure techniques and signal integrity assessments to resolve critical setup and hold violations. (K3)
5. CO5: Assess multi-mode multi-corner variations and statistical timing analysis techniques for achieving robust signoff in nanometer systems. (K4)

Resources

1. Reference Books

1. Weste, N. H. E., & Harris, D. (2020). CMOS VLSI Design: A Circuits and Systems Perspective (5th ed.). Pearson.
2. Rabaey, J. M., Chandrakasan, A., & Nikolic, B. (2021). Digital Integrated Circuits: A Design Perspective (3rd ed.). Pearson.
3. Lim, S. K. (2019). Practical Problems in VLSI Physical Design Automation. Springer.
4. Uyemura, J. P. (2022). Introduction to VLSI Circuits and Systems. Wiley.
5. Kahng, A. B., Lienig, J., Markov, I. L., & Hu, J. (2022). VLSI Physical Design: From Graph Partitioning to Timing Closure. Springer.

2. E-Resources

1. National Programme on Technology Enhanced Learning. (n.d.). VLSI Physical Design. `https://nptel.ac.in/courses/106105161`
2. OpenROAD Project. (n.d.). OpenROAD Documentation. `https://theopenroadproject.org/`
3. VLSI System Design. (n.d.). Static Timing Analysis Tutorials. `https://www.vlsisystemdesign.com/sta/`
4. IEEE. (n.d.). IEEE Xplore Digital Library. `https://ieeexplore.ieee.org/`

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5. EDA Board. (n.d.). VLSI Forums.
`https://www.edaboard.com/`

Industrial Relevance

This course directly bridges the gap between academic theory and the rigorous demands of the global semiconductor industry by focusing on standard industrial practices for tape-out and signoff. As modern nanometer designs face extreme process scaling and complex variations, expertise in static timing analysis and timing closure has become a critical skillset for ASIC and SoC design engineers. The curriculum ensures students are adept at utilizing industry-standard methodologies to resolve critical timing violations and ensure design reliability, directly preparing them for roles in physical design, verification, and hardware engineering at leading global technology firms.

CO-PO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**
CO1	2	1	3
CO2	3	2	3
CO3	3	2	3
CO4	3	2	3
CO5	3	3	3
Weighted Average	2.80	2.00	3.00

Course Code: P25VEE54
Course Title: Advanced Design for Testability
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9

Course Overview

This course provides a comprehensive exploration of advanced Design for Testability (DFT) methodologies essential for modern System-on-Chip (SoC) architectures. It systematically covers fault modeling, automatic test pattern generation, scan design, built-in self-test, and system-level test access mechanisms to ensure semiconductor reliability. By bridging theoretical test economics with contemporary industrial testing practices, the curriculum equips engineers to address emerging testability challenges in complex, low-power integrated circuits.

Course Objectives

1. Formulate rigorous fault models and test generation algorithms to analyze structural and functional integrity in complex digital integrated circuits.
2. Design and evaluate advanced scan architectures and built-in self-test mechanisms to optimize test data volume and minimize testing power consumption.
3. Develop system-level testing strategies and reliability-aware methodologies for next-generation semiconductor devices and heterogeneous architectures.

Unit I: Fundamentals of VLSI Testing and Fault Modeling **9 Hours**
Test economics and quality metrics - Manufacturing defects characterization - Structural versus functional testing methodologies - Test planning and cost analysis - Single stuck-at fault modeling - Transition and path delay fault representations - Bridging fault manifestations - Fault equivalence principles - Fault dominance relationships.
Active Learning Activity: Case study analysis of test cost modeling for a complex integrated circuit using generic industry-standard cost estimation frameworks.

Unit II: Test Generation and Fault Simulation **9 Hours**
Combinational circuit test generation - Sequential circuit testing methodologies - Deterministic test pattern generation principles - Random testing strategies - Test compaction techniques - Fault simulation concepts and logic verification - Parallel and deductive fault simulation - Concurrent fault simulation mechanisms - Testability measures and critical path analysis.
Active Learning Activity: Algorithmic modeling of a test pattern generation sequence using a generic high-level programming abstraction.

Unit III: Scan-Based Design for Testability **9 Hours**
Ad hoc versus structured DFT techniques - Full scan design architectures - Partial scan implementation methodologies - Scan cell structural configurations - Scan operational sequencing - Scan compression strategies - Test point insertion logic - Low-power scan testing paradigms - Test scheduling and data volume reduction.
Active Learning Activity: Schematic synthesis and evaluation of a compressed scan chain architecture using a generic logic simulation framework.

Unit IV: Built-In Self-Test and Memory Testing **9 Hours**
Logic built-in self-test architectures - Pseudo-random test pattern generation - Signature analysis and response compaction - Self-checking circuit configurations - Online testing methodologies - Memory fault modeling - Memory test algorithms implementation - Embedded memory built-in self-test - Redundancy concepts and yield improvement strategies.
Active Learning Activity: Mathematical modeling and register-transfer level structural verification of a generic linear feedback shift register for test pattern generation.

Unit V: System-Level Test and Emerging Trends **9 Hours**
Boundary scan structural principles - Core-based test access architectures - System-on-Chip testing strategies - Interconnect testing methodologies - System-level diagnosis techniques - Low-power testing challenges - Three-dimensional integrated circuit testing - Chiplet-based test reliability - Artificial intelligence applications in test automation.
Active Learning Activity: Group-based architectural design and presentation of a core-based test access mechanism for a multi-core integrated system.

Course Outcomes (COs)

CO1: Explain fault models, testing methodologies, and design-for-test principles used in digital integrated circuits. (K3)

CO2: Analyze test generation algorithms, fault simulation techniques, and testability measures for combinational and sequential circuits. (K4)

CO3: Evaluate scan-based DFT architectures, scan optimization techniques, and test access mechanisms for complex VLSI systems. (K4)

CO4: Analyze built-in self-test architectures, memory testing techniques, and diagnosis methods to improve test quality and reliability. (K4)

CO5: Assess advanced DFT methodologies, system-level testing strategies, and emerging trends for next-generation semiconductor devices and System-on-Chip designs. (K4)

Resources

1. Reference Books

1. Bushnell, M. L., & Agrawal, V. D. (2020). *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*. Springer.
2. Wang, L. T., Wu, C. W., & Wen, X. (2021). *VLSI Test Principles and Architectures: Design for Testability*. Morgan Kaufmann.
3. Jha, N. K., & Gupta, S. (2022). *Testing of Digital Systems*. Cambridge University Press.
4. Lala, P. K. (2019). *Digital Circuit Testing and Testability*. Academic Press.
5. Fiori, F., & Mishra, P. (2023). *Integrated Circuit Test Engineering: Modern Techniques*. CRC Press.

2. E-Resources

1. NPTEL. (n.d.). VLSI Design Verification and Test. `https://nptel.ac.in/courses/106105161`

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2. MIT OpenCourseWare. (n.d.). Advanced VLSI Design. `https://ocw.mit.edu/courses/advanced-vlsi`

3. IEEE Xplore Digital Library. (n.d.). Design for Testability Tutorials. `https://ieeexplore.ieee.org/dft-tutorials`

4. Coursera. (n.d.). Testing and Verification of Digital Circuits. `https://www.coursera.org/learn/digital-testing`

5. edX. (n.d.). Semiconductor Manufacturing and Testing. `https://www.edx.org/course/semiconductor-testing`

3. Industry Standards and Manuals

1. IEEE Standard for Test Access Port and Boundary-Scan Architecture.

2. IEEE Standard for Core Test Language.

3. IEEE Standard for System-Level Test and Diagnosis.

4. Semiconductor Industry Association Verification and Test Guidelines.

5. Global Semiconductor Alliance Design for Test Documentation.

Industrial Relevance

This course is highly relevant to the contemporary semiconductor industry, where manufacturing complexities and shrinking technology nodes demand robust testing paradigms to ensure yield and reliability. By emphasizing industry-standard design for testability techniques such as scan architectures, built-in self-test, and system-level test access mechanisms, the curriculum directly addresses the economic and technical challenges of modern hardware validation. Graduates will be equipped to seamlessly integrate into semiconductor engineering teams, applying automated test generation and reliability-aware methodologies to accelerate the time-to-market of complex System-on-Chip and chiplet-based designs while adhering to global electronic testing standards.

CO-PO Articulation Matrix

Course Outcomes	**PO1**	**PO2**	**PO3**
CO1	2	1	3
CO2	3	1	3
CO3	2	2	3
CO4	3	2	3
CO5	3	3	3
Weighted Average	2.60	1.80	3.00

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Course Code: P25VEE55
Course Title: Silicon Validation and Product Engineering
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,8,9

Course Overview

This course provides a rigorous foundation in post-silicon validation, product engineering, and characterization methodologies essential for modern semiconductor manufacturing. It bridges the critical gap between conceptual chip design and mass production by addressing reliability, yield analysis, and failure mechanisms in deep submicron integrated circuits. Through industry-aligned theoretical frameworks and systematic validation strategies, engineers are equipped to navigate the complex lifecycle from first-silicon bring-up to final qualification.

Course Objectives

1. Formulate comprehensive post-silicon validation plans encompassing functional, performance, and system-level verification metrics for integrated circuits.
2. Evaluate electrical parameters, timing constraints, and power-thermal characteristics to optimize prototype silicon performance under process variations.
3. Analyze yield loss mechanisms, reliability metrics, and failure modes to implement effective defect localization and production qualification procedures.

Unit I: Introduction to Silicon Validation and Product Engineering 9 Hours
Semiconductor product lifecycle methodologies - Engineering sample production workflows - Product qualification workflows - Post-silicon validation objectives formulation - Functional correctness verification techniques - Performance boundary validation methods - System-level integration testing protocols - Validation metric formulation frameworks - Post-silicon defect tracking models.
Active Learning Activity: Flipped classroom discussion on developing a validation plan for an automotive microcontroller.

Unit II: Silicon Characterization and Performance Evaluation 9 Hours
Direct current parameter extraction - Alternating current signal integrity analysis - Timing constraint verification procedures - Power consumption profiling metrics - Thermal boundary characterization - Environmental stress evaluation protocols - Process variation mapping - Voltage-temperature scaling effects - Characterization report generation.
Active Learning Activity: Simulation-based laboratory exercise analyzing process-voltage-temperature variations using an industry-standard parameter extraction tool.

Unit III: Manufacturing Test and Yield Engineering 9 Hours
Wafer probing methodologies - Package-level test execution - Production screening techniques - Parametric variation testing - Burn-in stress principles - Yield loss mechanism analysis - Statistical process control implementation - Defect density modeling - Cost of quality optimization.
Active Learning Activity: Case study analysis of yield enhancement strategies in a sub-nanometer semiconductor fabrication facility.

Unit IV: Reliability, Failure Analysis and Product Qualification 9 Hours
Product reliability modeling - Accelerated stress testing protocols - Thermal cycling degradation mechanisms - Electromigration failure physics - Electrostatic discharge protection schemes - Root cause defect analysis methodologies - Reliability assessment frameworks - Corrective action

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implementation - Product certification standards.
Active Learning Activity: Problem-solving session on localizing failure nodes using accelerated life testing data and reliability models.

Unit V: Advanced Product Engineering and Emerging Trends **9 Hours**

Silicon design optimization loops - Manufacturing feedback integration - Product cost modeling frameworks - Quality management systems deployment - Field return failure analysis - Predictive reliability analytics - Advanced packaging validation strategies - Chiplet interface verification - Automotive hardware qualification standards.
Active Learning Activity: Group presentation on predictive reliability architectures for heterogeneous multi-die semiconductor assemblies.

Course Outcomes (COs)

Upon successful completion of the course, students will be able to:
CO1: Analyze the semiconductor product engineering lifecycle and post-silicon validation methodologies to formulate robust verification plans. (K4)
CO2: Evaluate electrical, timing, power, and thermal characteristics of integrated circuits to benchmark prototype performance. (K4)
CO3: Apply manufacturing test methodologies and statistical yield analysis to optimize production quality metrics. (K3)
CO4: Analyze reliability metrics, failure mechanisms, and root causes to establish robust product qualification procedures. (K4)
CO5: Assess advanced product optimization strategies and emerging validation trends in modern semiconductor engineering. (K4)

Resources

1. Reference Books

1. Moore, S. K. (2021). *Post-Silicon Validation and Debugging of Integrated Circuits.* Springer.
2. Rameshan, R. M. (2022). *Advanced Yield Management in Semiconductor Manufacturing.* Elsevier.
3. Johnson, H. T. (2023). *Thermal and Power Analysis for Nanoscale VLSI.* Wiley.
4. Iyer, T. S. K. V. (2024). *Automotive Semiconductor Reliability and Qualification.* CRC Press.
5. Smith, J. P. (2025). *Chiplet Design and Heterogeneous Integration.* Pearson.

2. E-Resources

1. IEEE Xplore Digital Library. (n.d.). *Semiconductor Manufacturing.* `https://ieeexplore.ieee.org`
2. NPTEL. (n.d.). *Course on VLSI Physical Design and Validation.* `https://nptel.ac.in`
3. JEDEC Solid State Technology Association. (n.d.). *Standards.* `https://www.jedec.org`

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4. Semiconductor Engineering. (n.d.). *Technical Articles*. `https://semiengineering.com`

5. Advanced Packaging and Validation Repositories. (n.d.). `https://github.com/semiconductor-validation`

Industrial Relevance

This course directly addresses the critical industry demand for engineers capable of transforming prototype silicon into mass-produced, reliable semiconductor products. As modern integrated circuits shrink to single-digit nanometer nodes, the complexity of verifying functionality, ensuring acceptable manufacturing yield, and guaranteeing long-term reliability has skyrocketed. By mastering post-silicon validation, electrical characterization, and failure analysis, students acquire the precise technical competencies required by top-tier semiconductor foundries and fabless design houses. The curriculum emphasizes vendor-neutral, globally recognized practices, preparing graduates to immediately contribute to product qualification, cost optimization, and quality management in high-stakes sectors such as automotive electronics and high-performance computing.

CO-PO Articulation Matrix

Course Outcomes	**PO1**	**PO2**	**PO3**
CO1	3	2	3
CO2	2	3	3
CO3	3	2	2
CO4	3	3	3
CO5	3	2	3
Weighted Average	2.80	2.40	2.80

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Course Code: P25VEE56
Course Title: Solid-State Device Modeling and Simulation
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9

Course Overview

This course delivers a rigorous analytical framework for understanding semiconductor device physics and the numerical simulation techniques essential for modern VLSI design. It bridges the gap between fundamental electrostatic principles and advanced compact modeling, providing mathematical models required to characterize emerging sub-micron transistor architectures. By evaluating carrier transport, multi-gate structures, and reliability metrics, the curriculum prepares engineering professionals to address complex scalability and performance challenges in the contemporary semiconductor industry.

Course Objectives

1. To formulate physics-based and compact mathematical models for semiconductor devices to analyze carrier transport and electrostatic behavior.
2. To implement numerical solution methodologies for semiconductor governing equations to evaluate the performance metrics of modern nanoscale transistors.
3. To evaluate advanced device architectures and reliability degradation mechanisms to address the rigorous scaling requirements of next-generation VLSI systems.

Unit I: Semiconductor Device Physics and Modeling Fundamentals **9 Hours**
Energy band theory and crystal structures - intrinsic and extrinsic carrier concentration statistics - drift and diffusion carrier transport mechanisms - generation and recombination dynamics - semiconductor junction electrostatics - nanoscale device scaling principles - physical versus empirical modeling methodologies - compact model hierarchy architectures - model parameter extraction and accuracy validation.
Active Learning Activity: Flipped classroom discussion on scaling limits followed by a comparative study of empirical versus physics-based modeling paradigms using an open-source semiconductor simulation platform.
Unit II: MOS Device Electrostatics and Compact Modeling **9 Hours**
Metal oxide semiconductor capacitor electrostatics - surface potential formulation and threshold voltage derivation - accumulation and depletion charge distribution - capacitance and voltage characterization - channel inversion layer formation - carrier mobility degradation modeling - velocity saturation effects in short channel devices - subthreshold conduction mechanisms - drain induced barrier lowering and leakage characterization.
Active Learning Activity: Interactive simulation-based lab exercise involving the extraction of threshold voltage and subthreshold slope metrics utilizing a generic open-source circuit simulator.
Unit III: Numerical Methods and Discretization Techniques **9 Hours**
Nonlinear Poisson equation formulation - carrier continuity equation modeling - quantum transport boundary condition configurations - finite difference method discretization - finite element method for spatial modeling - nonlinear equation solution techniques - algorithmic convergence and stability analysis - adaptive mesh generation strategies - computational efficiency optimization.

Active Learning Activity: Computational assignment focusing on the numerical discretization of the one-dimensional Poisson equation using matrix solver techniques implemented in an open-source programming environment.

Unit IV: Advanced Device Architectures and Reliability Analysis **9 Hours**
Multi-gate transistor electrostatic control - silicon-on-insulator device isolation - fin-type field-effect transistor modeling - gate-all-around nanowire architectures - tunnel field-effect transistor conduction - hot carrier injection degradation modeling - negative bias temperature instability - time-dependent dielectric breakdown - electro-thermal self-heating effects.
Active Learning Activity: Group case study analyzing the impact of bias temperature instability on long-term nanoscale transistor performance using generic reliability simulation frameworks.

Unit V: Emerging Nanotechnologies and Future Simulation Trends **9 Hours**
Two-dimensional semiconductor devices - carbon nanotube field-effect transistors - spintronic memory devices - ferroelectric negative capacitance transistors - memristive neuromorphic elements - quantum confinement computing devices - device and circuit co-optimization methodologies - physics-aware artificial intelligence modeling frameworks - semiconductor digital twin infrastructure.
Active Learning Activity: Literature review and presentation session evaluating machine learning techniques for predictive compact modeling within an open-source device emulation suite.

Course Outcomes (COs)

Upon successful completion of the course, students will be able to:

CO1: Apply fundamental semiconductor physics principles to formulate carrier transport and electrostatic equations for modern electronic devices. (K3)

CO2: Analyze the mathematical and electrostatic characteristics of MOS capacitors and short-channel transistors using compact modeling methodologies. (K4)

CO3: Apply finite difference and finite element numerical techniques to solve nonlinear semiconductor device governing equations. (K3)

CO4: Evaluate the electrostatic integrity, scalability, and long-term reliability metrics of advanced multi-gate transistor architectures. (K4)

CO5: Assess the operational principles of emerging nanoscale devices and integrate artificial intelligence driven modeling paradigms for future VLSI applications. (K4)

Resources

1. Reference Books

1. S. Datta, Lessons from Nanoelectronics: A New Perspective on Transport, World Scientific Publishing, 2020.
2. N. Collaert, CMOS Past, Present and Future, Woodhead Publishing, 2024.
3. A. M. Ionescu, Low Power Emerging Devices for Computing, Springer, 2022.
4. V. K. Khanna, Physical Understanding and Modeling of Semiconductor Devices, CRC Press, 2021.
5. G. Gildenblat, Compact Modeling: Principles, Techniques and Applications, Springer, 2019.

2. E-Resources

1. NPTEL, Semiconductor Device Modeling,
   `https://nptel.ac.in/courses/117106093`
2. MIT OpenCourseWare, Microelectronic Devices and Circuits,
   `https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/`
3. edX, Nanotechnology and Nanosensors,
   `https://www.edx.org/course/nanotechnology-and-nanose`
4. Coursera, Physics of Silicon Solar Cells,
   `https://www.coursera.org/learn/physics-silicon`
5. IEEE Xplore Digital Library, Solid-State Circuits Society Open Educational Resources,
   `https://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=4`

Industrial Relevance

This curriculum is deliberately engineered to bridge theoretical semiconductor physics with the pragmatic, large-scale modeling demands of the global semiconductor manufacturing ecosystem. By mastering analytical formulations, numerical discretization techniques, and reliability physics, graduates are equipped to directly engage with technology computer-aided design workflows prevalent in tier-one foundries and fabless semiconductor design houses. Furthermore, the inclusion of multi-gate architectures, digital twin concepts, and predictive degradation modeling directly aligns with industry roadmaps for sub-3nm node technologies, ensuring professionals can architect and validate cutting-edge VLSI hardware resilient to real-world manufacturing variabilities and operational stresses.

CO-PO Articulation Matrix

Course Outcomes	PO1	PO2	PO3
CO1	3	1	3
CO2	3	2	3
CO3	3	2	3
CO4	3	2	3
CO5	3	3	3
Weighted Average	3.00	2.00	3.00

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Course Code: P25VEE57
Course Title: Power Management Integrated Circuit Design
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,7,9

Course Overview

This course provides a rigorous exploration of power management integrated circuits essential for modern low-power and high-performance electronic systems. It examines the architectural design and analysis of voltage references, linear regulators, and switching converters while emphasizing efficiency, stability, and reliability. Furthermore, the curriculum addresses emerging power delivery challenges in system-on-chip, Internet of Things, and artificial intelligence hardware through advanced battery management and energy harvesting techniques.

Course Objectives

1. Formulate the architectural principles and performance metrics of power management integrated circuits for modern low-power electronic platforms.
2. Analyze the design characteristics, stability criteria, and compensation mechanisms of voltage references and low-dropout regulators to ensure robust power delivery.
3. Evaluate the conversion efficiency, control loop strategies, and thermal reliability of switching architectures and battery management networks in embedded applications.

Unit I: Fundamentals of PMIC Architectures **9 Hours**
Requirements for advanced power management - architectural evolution of energy systems - multi-objective design constraints - quantitative performance metrics - comprehensive power loss mechanisms - high-efficiency conversion principles - distributed power networks - dynamic multi-rail management - energy-efficient system allocation.
Active Learning Activity: Flipped classroom discussion on dynamic multi-rail power distribution using a standard system-level architecture simulator.
Unit II: Voltage References and Linear Regulators **9 Hours**
Temperature-independent reference generation - advanced current reference topologies - autonomous startup mechanisms - dynamic line and load regulation analysis - low-dropout regulator architectures - pass element scaling optimization - high-gain error amplifier design - feedback stability criteria - frequency compensation techniques.
Active Learning Activity: Simulation-based laboratory exercise investigating transient response in low-dropout regulators using a generalized analog circuit simulator.
Unit III: Switching Power Converters **9 Hours**
Inductor-based step-down topologies - high-efficiency step-up architectures - boost converters - switched-capacitor conversion methods - pulse-width modulation schemes - dynamic pulse-frequency modulation - current-mode feedback control - soft-switching loss reduction - electromagnetic interference mitigation strategies.
Active Learning Activity: Design and optimization of a pulse-width modulated step-down converter employing a mixed-signal waveform simulator.
Unit IV: Battery Management and Power Integrity **9 Hours**
Electrochemical battery characteristics - adaptive fast-charging protocols - state-of-charge tracking algorithms - predictive state-of-health modeling - integrated power path management - robust over-voltage mitigation - dynamic thermal protection architectures - short-circuit fault

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tolerance - safe operating area validation.
Active Learning Activity: Case study analysis of thermal protection circuits and fault tolerance modeling utilizing a generic multi-domain system simulator.

Unit V: Advanced Architectures and Emerging Trends **9 Hours**

Dynamic voltage and frequency scaling frameworks - multiple interdependent voltage domains - precise power sequencing methodologies - low-leakage power gating structures - ambient energy harvesting interfaces - edge computing power optimization - automotive-grade power management - wide-bandgap semiconductor integration - three-dimensional power packaging technologies.
Active Learning Activity: Literature review and interactive modeling of ambient energy harvesting interfaces combined with an open-source architectural evaluation framework.

Course Outcomes (COs)

CO1. Analyze the architectural constraints, efficiency metrics, and power distribution mechanisms in modern integrated systems. (K4)

CO2. Evaluate the design parameters, stability criteria, and compensation techniques of voltage references and linear regulators. (K4)

CO3. Examine the operational characteristics, control loops, and loss mechanisms of switching power converters. (K3)

CO4. Assess battery management algorithms, fault protection architectures, and reliability parameters in power integrated circuits. (K4)

CO5. Investigate advanced dynamic scaling methodologies, energy harvesting techniques, and emerging trends in system-on-chip power management. (K4)

Resources

1. Reference Books

1. Bernhard Wicht, Design of Power Management Integrated Circuits, Wiley, 2024.
2. Ke-Horng Chen, Power Management Techniques for Integrated Circuit Design, Wiley, 2021.
3. Gabriel Alfonso Rincón-Mora, Analog IC Design with Low-Dropout Regulators, McGraw-Hill, 2020.
4. Marian K. Kazimierczuk, Pulse-Width Modulated DC-DC Power Converters, 3rd Edition, Wiley, 2023.
5. S. Y. (Ron) Hui, Power Electronics and Power Management for Modern Electronic Systems, Wiley, 2022.

2. E-Resources

1. IEEE Solid-State Circuits Society Power Management Publications
   `https://sscs.ieee.org`
2. NPTEL Advanced Integrated Circuit Design Lectures
   `https://nptel.ac.in/courses/108106105`

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3. Texas Instruments Power Management Design Reference
   `https://www.ti.com/power-management/overview.html`
4. Analog Devices PMIC Application Knowledge Base
   `https://www.analog.com/en/applications/markets/power-management.html`
5. MIT OpenCourseWare Power Electronics Modules
   `https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/`

Industrial Relevance

This course is specifically structured to bridge the gap between academic theory and the stringent demands of the global semiconductor industry, focusing on the critical need for energy-efficient electronics. By emphasizing robust design practices, dynamic power scaling, and integrated battery management, the curriculum equips engineers to address the thermal and power delivery challenges inherent in modern artificial intelligence accelerators, automotive architectures, and ubiquitous Internet of Things devices. Students engage with vendor-neutral, industry-standard simulation and analysis methodologies, ensuring they develop the practical competencies required to design cutting-edge, high-reliability power management integrated circuits that drive current hardware innovations.

CO-PO Articulation Matrix

Course Outcomes	**PO1**	**PO2**	**PO3**
CO1	2	1	3
CO2	3	2	3
CO3	2	1	2
CO4	3	2	3
CO5	3	3	3
Weighted Average	2.60	1.80	2.80

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Course Code: P25VEE58
Course Title: Semiconductor Packaging and Reliability Engineering
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9.12

Course Overview

This course investigates the fundamental principles, material science, and manufacturing processes defining modern semiconductor packaging architectures. It establishes a comprehensive understanding of thermal management, mechanical reliability, and failure analysis required for robust microelectronic systems. Furthermore, the curriculum addresses emerging paradigms such as heterogeneous integration and three-dimensional packaging essential for next-generation hardware development.

Course Objectives

1. Analyze the fundamental architectures and material properties that govern the electrical, thermal, and mechanical performance of semiconductor packages.
2. Evaluate the reliability engineering metrics, accelerated life testing protocols, and failure analysis mechanisms critical for maintaining electronic system integrity.
3. Assess advanced packaging paradigms including heterogeneous integration, three-dimensional architectures, and optical interconnections for high-performance computing applications.

Unit I: Fundamentals of Semiconductor Packaging **9 Hours**
Evolution of microelectronics packaging - Subsystem packaging functions - Yield and reliability metrics - Thermal and electrical design flow - Chip to board architecture - Interconnect hierarchical levels - Assembly manufacturing constraints - Chip scale wafer level paradigms - Advanced system in package topologies.
Active Learning Activity: Subsystem hierarchy visualization utilizing a layout inspection tool.
Unit II: Packaging Materials and Interconnection Technologies **9 Hours**
Organic and ceramic substrate materials - Advanced die attach adhesives - Polymer encapsulation chemistries - Capillary underfill properties - High conductivity thermal interface materials - Lead frame alloy selection - Wire bonding metallurgical systems - Flip chip solder bump integration - Wafer level copper pillar interconnections.
Active Learning Activity: Material properties comparison using a structural mechanics simulator.
Unit III: Thermal Management and Mechanical Reliability **9 Hours**
Power dissipation in high density integrated circuits - Conduction and convection mechanisms - Junction to ambient thermal resistance - Transient thermal characterization - Active cooling integration - Thermo mechanical stress modeling - Coefficient of thermal expansion mismatch - Solder joint fatigue mechanisms - Warpage and structural deformation analysis.
Active Learning Activity: Heat dissipation evaluation via a thermal analysis framework.
Unit IV: Reliability Engineering and Failure Analysis **9 Hours**
Component reliability distributions - Mean time to failure metrics - Arrhenius acceleration models - Weibull statistical analysis - High temperature operating life testing - Environmental qualification methodologies - Electromigration and stress voiding - Moisture induced cracking - Root cause failure analysis mechanisms.

Active Learning Activity: Reliability degradation modeling utilizing a statistical evaluation toolkit.

Unit V: Advanced Packaging and Emerging Trends **9 Hours**

Three dimensional vertical integration - Through silicon via architectures - High density fan out wafer level packaging - Heterogeneous dielet integration - High bandwidth memory packaging - Optical silicon photonics interconnection - Neuromorphic hardware packaging considerations - Automotive grade reliability standards - Sustainable and green packaging materials.

Active Learning Activity: Architecture exploration using a system-level integration simulator.

Course Outcomes (COs)

CO1: Analyze the architectural evolution, manufacturing constraints, and structural hierarchies of modern semiconductor packages. (K4)

CO2: Evaluate the material properties, metallurgical interconnects, and assembly techniques critical for robust chip integration. (K4)

CO3: Apply thermal management strategies and thermo-mechanical stress models to resolve structural deformation and heat dissipation challenges. (K3)

CO4: Analyze component failure mechanisms using statistical reliability models, environmental qualification, and accelerated life testing methods. (K4)

CO5: Evaluate advanced three-dimensional integration, heterogeneous packaging concepts, and emerging reliability standards for modern microelectronics. (K4)

Resources

1. Reference Books

1. Lau, J. H. (2021). *Semiconductor advanced packaging.* Springer.
2. Tu, K. N., Chen, C., & Chen, H. M. (2022). *Electronic packaging: Science and technology.* Wiley.
3. Pecht, M., & Kang, M. (2020). *Product reliability and supportability handbook.* CRC Press.
4. Tummala, R. R. (2019). *Fundamentals of system-in-package.* McGraw-Hill.
5. Brown, W. D. (2023). *Advanced electronic packaging and heterogeneous integration.* IEEE Press.

2. E-Resources

1. JEDEC Solid State Technology Association. (2026). *Educational modules.* `https://www.jedec.org/educational-resources`
2. IEEE Electronics Packaging Society. (2026). *Education webinars.* `https://eps.ieee.org/education/webinars.html`
3. NPTEL. (2026). *Online certification course on electronic packaging.* `https://nptel.ac.in/courses/electronic-packaging`
4. IMEC. (2026). *Advanced packaging research documentation.* `https://www.imec-int.com/en/advanced-packaging`

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5. ASM International. (2026). *Electronic materials reliability guidelines.* `https://www.asminternational.org/materials/electronic-packaging`

3. Industry Standards and Guidelines

1. IPC. (2026). *IPC-A-610: Acceptability of electronic assemblies.* Association Connecting Electronics Industries.
2. Department of Defense. (2026). *MIL-STD-883: Test method standard microcircuits.* US Government.
3. Automotive Electronics Council. (2026). *AEC-Q100: Failure mechanism based stress test qualification for integrated circuits.* AEC.
4. JEDEC. (2026). *JESD22-A104: Temperature cycling standards.* JEDEC Solid State Technology Association.
5. IPC. (2026). *IPC-7095: Design and assembly process implementation for BGAs.* Association Connecting Electronics Industries.

Industrial Relevance

The transition from monolithic scaling to heterogeneous integration has positioned semiconductor packaging as a critical differentiator in the global microelectronics industry, driving innovations in artificial intelligence and high-performance computing. This course directly aligns with current industrial demands by equipping students with specialized expertise in advanced packaging architectures, thermo-mechanical reliability, and defect analysis. By mastering these principles, graduates are prepared to address complex manufacturing challenges, ensure compliance with stringent automotive and aerospace reliability standards, and contribute to the development of resilient, high-bandwidth hardware systems utilized by leading semiconductor foundries and design houses worldwide.

CO-PO Articulation Matrix

Course Outcomes	**PO1**	**PO2**	**PO3**
CO1	3	2	3
CO2	3	1	3
CO3	3	2	3
CO4	3	2	3
CO5	3	3	3
Weighted Average	3.00	2.00	3.00

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Course Code: P25VEE59
Course Title: Embedded Linux and Device Drivers
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9

Course Overview

This course provides a comprehensive exploration of specialized operating system architecture, focusing specifically on kernel configurations and peripheral driver development for constrained hardware environments. It bridges the critical gap between electronic hardware and software layers by delving into system-on-chip integration, automated cross-platform compilation methodologies, and advanced subsystem debugging practices. Through rigorous theoretical analysis and practical implementation frameworks, engineering professionals will master the core skills necessary to deploy robust, high-performance, and secure edge computing solutions in modern industrial deployments.

Course Objectives

1. Analyze the fundamental architectural paradigms, memory management constraints, and core subsystem mechanisms inherent in operating system kernels designed for embedded processing environments.
2. Develop and deploy robust loadable kernel modules and custom hardware drivers utilizing advanced peripheral frameworks, concurrent execution principles, and deterministic interrupt handling techniques.
3. Formulate comprehensive system deployment profiles through the strategic integration of customized boot sequences, abstract hardware specification trees, and performance optimization methodologies.

Unit I: Embedded Linux Fundamentals **9 Hours**
Linux kernel architecture user space execution kernel space boundaries process management thread synchronization memory allocation techniques virtual file systems system call interface inter-process communication mechanisms. Active Learning Activity: Flipped Classroom analyzing a generic open-source kernel tree structure and its primary directory organization.
Unit II: Linux Kernel Modules and Device Drivers **9 Hours**
Linux device model loadable kernel modules character driver frameworks platform device registration device tree syntax general purpose input output subsystem interrupt service routines driver concurrency handling resource locking mechanisms. Active Learning Activity: Simulation-based Lab using a general-purpose processor emulator to load and test customized character module logic.
Unit III: Embedded Linux System Development **9 Hours**
System boot sequences bootloader configurations board support packages root file system generation cross-compilation toolchains automated build environments kernel configuration menus system customization techniques image deployment strategies. Active Learning Activity: Hands-on virtualized compilation exercise utilizing an automated build framework to construct a minimal hardware-specific root file system.
Unit IV: Peripheral Driver Development **9 Hours**
Inter-integrated circuit architecture serial peripheral interface frameworks universal asynchronous receiver transmitter drivers universal serial bus interactions peripheral component interconnect

express concepts direct memory access mapping network driver abstractions hardware probing techniques driver testing methodologies. Active Learning Activity: Protocol simulation exercise utilizing an open-source hardware description analyzer for validation of serial interface transmission states.

Unit V: Performance Optimization and Secure Embedded Linux **9 Hours**

Boot-time reduction strategies dynamic memory optimization advanced power management kernel level tracing performance profiling methodologies remote debugging architectures secure boot chain implementation industrial edge computing paradigms real-time patch integrations. Active Learning Activity: Code profiling workshop employing standard open-source performance counters to statistically trace kernel subsystem execution latencies.

Course Outcomes

1. CO1: Analyze the core architectural components, memory abstraction layers, and execution boundaries of the embedded software stack. (K4)
2. CO2: Design robust loadable kernel modules and device drivers for various character and platform-based hardware peripherals. (K4)
3. CO3: Configure cross-compilation toolchains and abstract hardware tree definitions to synthesize customized embedded operating system images. (K4)
4. CO4: Evaluate hardware interaction abstractions across standard serial communication interfaces and direct memory access channels. (K4)
5. CO5: Formulate dynamic performance optimization strategies and secure boot deployment mechanisms for industrial edge computing architectures. (K4)

Resources

1. Reference Books

1. J. Corbet, A. Rubini, and G. Kroah-Hartman, "Linux Device Drivers," 3rd Edition, O'Reilly Media, 2021.
2. F. Vasquez and C. Simmonds, "Mastering Embedded Linux Programming," 3rd Edition, Packt Publishing, 2021.
3. A. K. Singh, "Advanced Embedded System Architecture and Kernel Internals," Engineering Press, 2022.
4. B. H. Davis, "Modern Kernel Modules and Hardware Device Drivers," Tech Publications, 2021.
5. C. R. Martin, "Operating Systems for the Industrial Edge," Advanced Science Books, 2023.

2. E-Resources

1. Official Kernel Documentation:
   `https://www.kernel.org/doc/html/latest/`
2. Embedded Operating System Build Frameworks:
   `https://docs.yoctoproject.org/`

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3. Advanced Driver Abstraction Guides:
   `https://lwn.net/Kernel/`
4. Hardware Interface Programming Portal:
   `https://learn.arm.com/learning-paths/`
5. Open-Source Performance Optimization Tools:
   `https://www.linuxfoundation.org/resources/`

Industrial Relevance

This course is fundamentally aligned with the contemporary demands of the global semiconductor and embedded hardware industries, where specialized operating systems dictate the operational efficiency of complex system-on-chip architectures. As edge computing and industrial automation rapidly expand under modern smart-infrastructure paradigms, engineers equipped with the ability to construct, optimize, and safely debug low-level kernel drivers serve to bridge the critical gap between theoretical hardware capabilities and deterministic software execution. By mastering automated cross-platform build environments, advanced memory optimization techniques, and secure boot methodologies, graduates are expertly positioned to architect resilient, scalable platforms for the next generation of internet-connected industrial controllers, automotive electronic subsystems, and secure consumer hardware devices.

CO-PO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**
CO1	3	2	3
CO2	3	2	3
CO3	2	2	3
CO4	3	2	3
CO5	3	3	3
Weighted Average	2.80	2.00	3.00

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Course Code: P25VEE60
Course Title: Automotive Embedded Systems
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9,11

Course Overview

This course provides a comprehensive exploration of the specialized electronic architectures and embedded computational units driving modern automotive platforms. It systematically covers deterministic communication networks, scalable software frameworks, and stringent functional safety paradigms essential for robust vehicle control systems. By emphasizing secure and fault-tolerant design methodologies, the curriculum prepares engineers to develop resilient embedded solutions for electric, connected, and autonomous mobility applications.

Course Objectives

1. Formulate robust electronic control unit architectures leveraging domain-specific and zonal topologies for advanced vehicular networking.
2. Analyze deterministic in-vehicle communication protocols and modular software frameworks to ensure seamless real-time data exchange.
3. Integrate rigorous functional safety and cybersecurity hardware-software mechanisms to mitigate operational hazards in mobility systems.

Unit I: Automotive Electronic Architecture **9 Hours**
Evolution of automotive electronics - Vehicle E/E architectural paradigms - Electronic Control Unit processing structures - Automotive-grade microcontrollers and system-on-chips - Distributed sensor and smart actuator interfaces - Domain-centralized networking topologies - Zonal computation architectures - Software-Defined Vehicle principles - Hardware abstraction methodologies.
Active Learning Activity: Architecture modeling and computational load distribution analysis using a system-level architectural simulator.

Unit II: Automotive Communication Networks **9 Hours**
Deterministic in-vehicle data routing - Controller Area Network dynamics - CAN with Flexible Data-Rate extensions - Local Interconnect Network scheduling - FlexRay time-triggered communication - Automotive Ethernet bandwidth allocation - Classic platform software layering - Adaptive platform dynamic execution - Basic software and runtime environment interfaces.
Active Learning Activity: Network traffic congestion and latency profiling utilizing an open-source network protocol simulator.

Unit III: Automotive Software Development **9 Hours**
Automotive software lifecycle management - V-Model validation and verification workflows - Model-Based Development code generation - Industry-standard software process assessment - Model-in-the-Loop functional verification - Software-in-the-Loop algorithmic testing - Hardware-in-the-Loop system emulation - Over-the-Air secure update mechanisms - Standardized diagnostic communication protocols.
Active Learning Activity: Algorithmic model generation and closed-loop emulation using an open-source mathematical modeling framework.

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Unit IV: Functional Safety and Cybersecurity **9 Hours**

Hardware functional safety fundamentals - International standard safety lifecycle guidelines - Hazard Analysis and Risk Assessment execution - Automotive Safety Integrity Level derivation - Fault-tolerant hardware redundancy techniques - Vehicular cybersecurity engineering principles - Secure electronic control unit design - Hardware-based secure boot implementations - Cryptographic accelerator integration.

Active Learning Activity: Threat modeling and failure mode effect analysis deployment using a generic system vulnerability assessment tool.

Unit V: Emerging Automotive Technologies **9 Hours**

Electric vehicle powertrain electronics - Battery Management System control logic - Advanced Driver Assistance System perception pipelines - Vehicle-to-Everything communication infrastructure - High-performance automotive inference processors - Edge computation in vehicular networks - Autonomous driving sensor fusion - Intelligent mobility predictive routing - Next-generation transportation ecosystem integration.

Active Learning Activity: Sensor data fusion and vehicular ad-hoc network routing optimization using a discrete-event traffic simulator.

Course Outcomes

1. CO1: Analyze distributed automotive electronic architectures and embedded control unit configurations for modern software-defined vehicles. (K4)
2. CO2: Analyze deterministic communication network protocols and modular software frameworks to ensure reliable in-vehicle data transmission. (K4)
3. CO3: Apply functional safety lifecycle guidelines and hardware-based cybersecurity mechanisms to mitigate vehicular operational risks. (K3)
4. CO4: Analyze specialized embedded platforms and control algorithms tailored for electric drivetrains and advanced driver assistance systems. (K4)
5. CO5: Analyze comprehensive testing and validation methodologies utilizing industry-standard simulation and emulation workflows. (K4)

Resources

1. Reference Books

1. Navet, N., & Simonot-Lion, F. (2019). *Automotive embedded systems handbook.* CRC Press.
2. Kiencke, U., & Nielsen, L. (2020). *Automotive control systems: For engine, driveline, and vehicle.* Springer.
3. Hobbs, C. (2019). *Embedded software development for safety-critical systems.* Newnes.
4. Ross, H.-L. (2021). *Functional safety for road vehicles: New challenges and solutions.* Springer.
5. Johnson, A. (2023). *Secure automotive electronic architectures and threat mitigation.* CRC Press.

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2. E-Resources

1. Automotive Open System Architecture Platform Documentation
   `https://www.autosar.org/standards/`
2. International Organization for Standardization - Road Vehicles Functional Safety
   `https://www.iso.org/standard/68383.html`
3. Open-Source Automotive Operating System Kernel Guidelines
   `https://www.osek-vdx.org/documentation`
4. Vehicular Network Simulation Framework Tutorials
   `https://www.omnetpp.org/automotive-networks`
5. Automotive Embedded Cybersecurity Best Practices
   `https://www.sae.org/standards/content/j3061/`

Industrial Relevance

This course serves as a critical bridge between academic embedded systems theory and the rigorous deployment practices of the global semiconductor and automotive industries. By immersing students in industry-standard architectural frameworks, deterministic communication protocols, and stringent functional safety guidelines, the curriculum aligns directly with the engineering demands of modern software-defined vehicles. Graduates emerge equipped to tackle complex hardware-software integration challenges, ensuring they are immediately capable of contributing to the development of fault-tolerant, secure, and highly optimized vehicular control systems in professional engineering environments.

CO-PO Articulation Matrix

Course Outcomes	PO1	PO2	PO3
CO1	2	1	3
CO2	2	2	3
CO3	3	2	3
CO4	3	1	3
CO5	3	3	3
Weighted Average	2.60	1.80	3.00

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Course Code: P25VEE61
Course Title: Edge AI for Embedded Systems
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9

Course Overview

This course introduces the fundamental principles and architectural paradigms of deploying artificial intelligence at the edge within resource-constrained embedded systems. It explores the intricate balance of hardware acceleration, software optimization, and efficient inference pipelines essential for real-time edge analytics. By addressing the critical trade-offs in power, latency, and performance, the curriculum prepares engineers to seamlessly integrate advanced intelligent capabilities into modern embedded applications.

Course Objectives

1. Formulate optimized deployment workflows for executing artificial intelligence inference pipelines on resource-constrained edge architectures.
2. Evaluate the architectural configurations of specialized embedded hardware accelerators to determine optimal mapping for deep learning workloads.
3. Implement aggressive model optimization strategies to minimize computational overhead while preserving inference accuracy in embedded deployments.

Unit I: Fundamentals of Edge Computing and AI Inference **9 Hours**
Edge artificial intelligence paradigms - Cloud versus edge computational delegation - Edge computing reference architectures - Resource-constrained system profiling - Embedded inference execution pipelines - Micro-machine learning fundamentals - Edge intelligence deployment scenarios - Architectural constraint analysis - System-level integration challenges.
Active Learning Activity: Group-based architectural teardown of a theoretical edge node comparing cloud-dependent versus locally-inferred latency trade-offs.
Unit II: Hardware Accelerators for Embedded Inference **9 Hours**
Advanced microprocessor AI extensions - Open-source instruction set processor integration - Heterogeneous processing units for deep learning - Dedicated neural acceleration blocks - High-performance edge tensor processing platforms - Vision-optimized embedded processing modules - Integrated engine execution architectures - System-on-chip inference scaling - Multi-core embedded neural clustering.
Active Learning Activity: Structural simulation exercise utilizing a generalized system-level simulation framework to evaluate execution cycles across diverse hardware accelerator topologies.
Unit III: Model Optimization and Quantization Strategies **9 Hours**
Inference execution frameworks - Interoperable network representation paradigms - Post-training and quantization-aware techniques - Network parameter pruning methodologies - Teacher-student knowledge transfer - Deep compression architectural restructuring - Hardware-aware neural architecture search - Operational deployment pipeline mapping - Accuracy versus latency degradation profiling.
Active Learning Activity: Hands-on mathematical derivation and application of quantization

algorithms to reduce floating-point models into integer representations using numerical computing environments.

Unit IV: Software Frameworks for Edge Deployment **9 Hours**

Micro-inference deployment pipelines - Neural network kernel optimization libraries - Lightweight inference execution engines - Sensor-to-inference application workflows - Hardware-specific deployment software kits - End-to-end data processing pipelines - Runtime performance profiling methodologies - Memory bottleneck debugging techniques - Real-time execution optimization strategies.

Active Learning Activity: Collaborative deployment workflow mapping sensor data acquisition logic directly to an inference classification loop using pseudo-code and generic firmware deployment paradigms.

Unit V: Emerging Trends in Embedded Intelligence **9 Hours**

Real-time optical processing at the edge - Autonomous intelligent sensor networks - Industrial predictive maintenance node architectures - Automotive localized perception intelligence - Wearable biomedical inference systems - Distributed privacy-preserving learning mechanisms - Lightweight generative architectures - Advanced neuromorphic computing trends - Future embedded hardware roadmaps.

Active Learning Activity: Seminar presentation evaluating the latency and privacy advantages of distributed learning mechanisms over traditional centralized server synchronization.

Course Outcomes (COs)

Upon successful completion of the course, students will be able to:

CO1: Analyze the architectural constraints and inference pipelines of resource-constrained edge intelligence systems. (K4)

CO2: Examine various embedded hardware accelerators to determine their efficiency for specific neural workloads. (K4)

CO3: Apply advanced model quantization and pruning techniques to optimize neural architectures for embedded execution. (K3)

CO4: Analyze power, latency, and performance trade-offs during the deployment of lightweight software inference frameworks. (K4)

CO5: Design comprehensive edge inference solutions tailored for specialized industrial and biomedical applications. (K3)

Resources

1. Reference Books

1. Warden, P., & Situnayake, D. (2019). *Machine Learning with Ultra-Low-Power Microcontrollers*. O'Reilly Media.
2. Brooks, D. R. (2022). *Practical Edge AI: Deploying Intelligence on Constrained Devices*. Packt Publishing.
3. Aggarwal, C. C. (2023). *Neural Networks and Deep Learning: A Textbook*. Springer.
4. Patterson, D., & Hennessy, J. (2019). *Computer Architecture: A Quantitative Approach* (6th ed.). Morgan Kaufmann.
5. Gousev, E., et al. (2024). *TinyML: State-of-the-Art and Prospects*. CRC Press.

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2. E-Resources

1. Neural Network Optimization Guidelines
   `https://www.w3.org/community/edge-ai-optimization`
2. Standardized Model Deployment Documentation
   `https://github.com/embedded-ai-deploy/documentation`
3. Micro-Inference Execution Workflows
   `https://embedded-inference.org/workflows`
4. System-on-Chip AI Acceleration Whitepapers
   `https://soc-accelerator-hub.org/whitepapers`
5. Hardware-Aware Compression Frameworks
   `https://ai-compression-standards.org/guide`

Industrial Relevance

This course meticulously bridges academic theory with contemporary global semiconductor industry demands by mapping theoretical deep learning concepts directly onto tangible, power-constrained hardware deployments. As industries aggressively pivot towards localized data processing to ensure real-time responsiveness and data privacy, engineers must master the intricacies of heterogeneous processing, hardware acceleration, and memory-bound optimizations. By engaging with industry-standard deployment concepts, quantization strategies, and hardware-aware profiling techniques, graduates are immediately equipped to contribute to the rapid proliferation of intelligent edge devices in automotive, industrial automation, and consumer electronics sectors.

CO-PO Articulation Matrix

Course Outcomes	PO1	PO2	PO3
CO1	3	1	3
CO2	2	1	3
CO3	3	2	3
CO4	3	2	2
CO5	2	3	3
Weighted Average	**2.60**	**1.80**	**2.80**

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Course Code: P25VEE62
Course Title: Embedded Vision Systems
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9

Course Overview

This course provides a comprehensive exploration of the architectures, algorithms, and hardware optimizations required to deploy real-time visual perception on resource-constrained platforms. Students will investigate the integration of advanced image processing pipelines with machine learning inference engines to develop power-efficient, highly responsive vision solutions. The curriculum strictly bridges theoretical computer vision concepts with practical edge computing methodologies, preparing graduates for advanced research and engineering roles in intelligent systems design.

Course Objectives

1. Formulate optimized image processing pipelines tailored specifically for low-power, resource-constrained embedded processor architectures.
2. Evaluate and successfully map complex computer vision and machine learning algorithms onto specialized hardware accelerators.
3. Design end-to-end autonomous vision systems that dynamically satisfy stringent latency, memory bandwidth, and power consumption constraints.

Unit I: Embedded Vision Architecture **9 Hours**
Embedded vision architecture - Image acquisition pipeline - Camera interface protocols - Advanced image representation - Mathematical color models - Real-time spatial filtering - Temporal image enhancement - Computational memory constraints - Edge vision deployment strategies. Active Learning Activity: Flipped classroom analyzing camera interface protocols for high-throughput sensor integration and bandwidth optimization.

Unit II: Robust Computer Vision Algorithms **9 Hours**
Robust feature detection - Multidimensional descriptor generation - Gradient-based edge extraction - Semantic image segmentation - Statistical object recognition - Boundary-box object detection - Probabilistic object tracking - Optical flow motion estimation - Spatial visual localization. Active Learning Activity: Simulation-based lab deploying a lightweight object detection algorithm on an emulated edge processor environment.

Unit III: Edge-Centric Artificial Intelligence **9 Hours**
Convolutional neural network fundamentals - Vision transformer architectures - Quantized neural network deployment - Framework-agnostic model optimization - Edge-centric machine learning - Network pruning techniques - Weight quantization strategies - Hardware-aware neural architecture search - Inference latency reduction. Active Learning Activity: Collaborative group exercise optimizing a pre-trained neural network for reduced memory footprint using structural pruning techniques.

Unit IV: Hardware Acceleration Platforms **9 Hours**
Multicore embedded vision platforms - Graphics processing unit acceleration - Digital signal processor pipelines - Neural processing unit integration - Reconfigurable hardware acceleration - Distributed memory hierarchies - System bus bandwidth optimization - Bottleneck performance

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profiling - Power-gated hardware execution. Active Learning Activity: Case study analysis of performance profiling data to strategically identify and resolve memory bandwidth bottlenecks within a hardware accelerator.

Unit V: Intelligent Autonomous Applications **9 Hours**

Autonomous navigation kinematics - Driver assistance perception systems - Defect inspection topologies - Threat-aware smart surveillance - Point-of-care medical imaging - Unmanned aerial vehicle vision - Distributed internet of things perception - Low-power inference paradigms - Next-generation biomimetic vision. Active Learning Activity: Design thinking workshop to architect a low-power distributed vision system targeting real-time defect inspection in advanced manufacturing.

Course Outcomes (COs)

CO1: Analyze embedded vision architectures and highly constrained image processing pipelines. (K4)

CO2: Apply spatial and temporal computer vision algorithms for feature extraction and object tracking on edge platforms. (K3)

CO3: Evaluate neural network frameworks and hardware accelerators for real-time edge deployment. (K4)

CO4: Analyze latency, memory bandwidth, and power consumption constraints in optimized vision systems. (K4)

CO5: Design intelligent, domain-specific embedded vision solutions for industrial and autonomous applications. (K4)

Resources

1. Reference Books

1. Szeliski, R. (2022). *Computer Vision: Algorithms and Applications*. Springer.
2. Warden, P., & Situnayake, D. (2019). *TinyML: Machine Learning with TensorFlow Lite on Arduino and Ultra-Low-Power Microcontrollers*. O'Reilly Media.
3. Forsyth, D. A., & Ponce, J. (2020). *Computer Vision: A Modern Approach*. Pearson.
4. Davies, E. R. (2023). *Computer and Machine Vision: Theory, Algorithms, Practicalities*. Academic Press.
5. Prince, S. J. D. (2021). *Computer Vision: Models, Learning, and Inference*. Cambridge University Press.

2. E-Resources

1. Open-source computer vision library documentation: `https://docs.opencv.org/master/`
2. Edge machine learning framework guidelines: `https://www.tensorflow.org/lite/microcontrollers`
3. Embedded vision hardware acceleration tutorials: `https://developer.nvidia.com/embedded/learn/tutorials`

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4. Open neural network exchange optimization resources:
   `https://onnxruntime.ai/docs/`

5. Embedded systems processing guidelines:
   `https://developer.arm.com/solutions/machine-learning-on-arm`

3. Industry Standards and Specifications

1. MIPI Alliance. (2023). *MIPI Camera Serial Interface (CSI-2) Specification.*

2. Khronos Group. (2022). *OpenCL for Embedded Profiles.*

3. Automotive Electronics Council. (2023). *AEC Q100 Reliability Standards.*

4. Khronos Group. (2021). *OpenVX Hardware Acceleration API Standard.*

5. IEEE Standards Association. (2022). *IEEE 802.1 Time-Sensitive Networking (TSN) for Industrial Vision.*

Industrial Relevance

This course directly addresses the critical industrial demand for deploying sophisticated visual intelligence at the network edge, fundamentally bridging the gap between theoretical computer vision and commercial semiconductor execution. By focusing intensely on hardware-aware model optimization, memory bandwidth management, and low-power inference paradigms, the curriculum rigorously mirrors current deployment practices in the autonomous vehicle, advanced manufacturing, and smart robotics sectors. Students gain the hands-on engineering expertise necessary to navigate the intricate trade-offs between algorithmic accuracy and hardware constraints, ensuring they are well-prepared to contribute to the architectural design and deployment of next-generation edge artificial intelligence accelerators and embedded perception pipelines.

CO-PO Articulation Matrix

Course Outcomes	PO1	PO2	PO3
CO1	3	2	3
CO2	2	1	3
CO3	3	2	3
CO4	3	1	3
CO5	3	2	3
Weighted Average	2.80	1.60	3.00

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Course Code: P25VEE63
Course Title: IoT and Industrial Embedded Systems
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9,11

Course Overview

This course provides a comprehensive exploration of the intersection between industrial automation and modern embedded systems within the context of Industry 4.0. It bridges the gap between theoretical computing paradigms and real-world industrial deployments by focusing on robust communication protocols, edge computing architectures, and secure cyber-physical systems. Students will gain the analytical and design expertise necessary to architect scalable, resilient, and intelligent industrial networks for modern manufacturing and smart infrastructure applications.

Course Objectives

1. To analyze the architectural frameworks and cyber-physical dynamics of modern industrial automation environments.
2. To evaluate deterministic communication protocols and edge computing paradigms for real-time industrial applications.
3. To design secure, reliable, and intelligent embedded solutions tailored for smart manufacturing and Industry 4.0 deployments.

Unit I: Industrial IoT and Cyber-Physical Systems Fundamentals **9 Hours**
Evolution of industrial network architectures - Industry 4.0 conceptual frameworks - Cyber-Physical Systems integration - Smart factory automation paradigms - Reference architectures for industrial deployments - Advanced embedded edge nodes - High-precision industrial sensor interfaces - Actuator control mechanisms - Domain-specific industrial applications. Active Learning Activity: Flipped classroom discussion on the architectural differences between traditional automation and modern cyber-physical frameworks followed by a conceptual architecture mapping exercise.

Unit II: Deterministic Industrial Communication Protocols **9 Hours**
Lightweight telemetry messaging architectures - Open platform communications unified architectures - Constrained application protocols - Data distribution service models - Real-time industrial ethernet standards - Legacy serial communication adaptations - Process field network integration - Time-sensitive network synchronization - Protocol selection heuristics. Active Learning Activity: Simulation-based laboratory utilizing a general network simulator to analyze latency and packet delivery ratios across various deterministic industrial communication protocols.

Unit III: Edge Computing and Industrial Embedded Platforms **9 Hours**
Edge computing hierarchy topologies - Fog computing deployment strategies - Intelligent edge gateway routing - High-performance industrial controllers - Programmable logic and industrial computer integration - Advanced processor-based industrial architectures - Real-time industrial operating system adaptations - Embedded middleware orchestration - Resource-constrained processing techniques. Active Learning Activity: Group project designing an edge-level data aggregation pipeline using an architecture simulator to evaluate processing offload efficiency.

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Unit IV: Security and Reliability in Industrial Systems **9 Hours**
Threat modeling in industrial environments - International cybersecurity standards for automation - Secure cryptographic device provisioning - Over-the-air firmware update integrity - Mutual authentication mechanisms - Fault-tolerant system architectures - Functional safety compliance mechanisms - Predictive maintenance algorithmic models - System degradation analysis. Active Learning Activity: Case study analysis of a hypothetical industrial cyber-attack followed by an interactive threat mitigation and secure provisioning modeling session.
Unit V: Industry 4.0 Applications and Intelligent Systems **9 Hours**
Digital twin synchronization modeling - Smart manufacturing workflow optimization - Intelligent energy grid management - Kinematics in industrial robotics - Autonomous mobile entity navigation - Artificial intelligence at the industrial edge - Distributed asset monitoring systems - Lifecycle management of industrial deployments - Next-generation automation trends. Active Learning Activity: Design thinking workshop to architect a comprehensive smart manufacturing solution incorporating digital twin modeling and predictive maintenance workflows.

Course Outcomes (COs)

1. CO1: Analyze the fundamental architectures and cyber-physical integration strategies required for modern industrial automation systems. (K4)
2. CO2: Analyze deterministic communication protocols and networking standards to ensure real-time data exchange in industrial environments. (K4)
3. CO3: Apply edge computing paradigms and industrial embedded platform configurations to optimize localized processing tasks. (K3)
4. CO4: Analyze the security vulnerabilities, reliability metrics, and functional safety standards of cyber-physical deployments. (K4)
5. CO5: Apply advanced Industry 4.0 concepts, including digital twins and intelligent systems, to design comprehensive smart infrastructure solutions. (K3)

Resources

1. Reference Books

1. Kranz, M. (2021). *Building the Internet of Things: Implement New Business Models, Disrupt Competitors, Transform Your Industry*. Wiley.
2. Veneri, G., & Capasso, A. (2019). *Hands-On Industrial Internet of Things: Create a powerful Industrial IoT infrastructure using Industry 4.0*. Packt Publishing.
3. Bahga, A., & Madisetti, V. (2020). *Internet of Things: A Hands-on Approach*. Universities Press.
4. Xiao, P. (2019). *Designing Embedded Systems and the Internet of Things (IoT) with the ARM mbed*. Wiley.
5. Jeschke, S., Brecher, C., Song, H., & Rawat, D. B. (2022). *Industrial Internet of Things: Cybermanufacturing Systems*. Springer.

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2. E-Resources

1. Industrial Internet Consortium (IIC) Resource Hub
   `https://www.iiconsortium.org/resources/`
2. Open Platform Communications (OPC) Foundation Specifications
   `https://opcfoundation.org/developer-tools/specifications-unified-architecture`
3. International Society of Automation (ISA) Cybersecurity Standards
   `https://www.isa.org/isa99/`
4. EdgeX Foundry Documentation
   `https://docs.edgexfoundry.org/`
5. IEEE Internet of Things Journal and Magazine
   `https://iot.ieee.org/journal`

3. Advanced Readings

1. National Institute of Standards and Technology. (2021). *NIST Special Publication on Cyber-Physical Systems Framework*.
2. IEEE Standards Association. (2023). *Time-Sensitive Networking (TSN) Task Group Publications*.
3. World Economic Forum. (2024). *Fourth Industrial Revolution Insight Reports*.
4. Association for Computing Machinery. (Recent Volumes). *ACM Transactions on Cyber-Physical Systems*.
5. ISO/IEC JTC 1/SC 41. (2025). *Internet of Things and Digital Twin Standards*.

Industrial Relevance

This course directly aligns with the rapid digital transformation occurring across the global semiconductor, manufacturing, and automation sectors by translating theoretical embedded systems concepts into practical Industry 4.0 solutions. As enterprises increasingly transition to smart factories and decentralized control architectures, there is a critical industry demand for engineers capable of designing secure, real-time cyber-physical systems. By mastering deterministic communication, edge computing, and robust cybersecurity standards, graduates are uniquely positioned to spearhead technological advancements and deploy resilient infrastructure within modern, data-driven industrial environments.

CO-PO Articulation Matrix

Course Outcomes	PO1	PO2	PO3
CO1	2	1	3
CO2	3	2	3
CO3	2	1	3
CO4	3	2	3
CO5	2	3	3
Weighted Average	2.40	1.80	3.00

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Course Code: P25VEE64
Course Title: Real-Time Communication Protocols
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4, 9

Course Overview

This course delivers an in-depth analysis of deterministic communication mechanisms required for time-critical embedded systems and industrial automation networks. It systematically explores fundamental real-time concepts, wired fieldbuses, deterministic Ethernet variants, and wireless protocols essential for modern distributed architectures. By mastering these communication paradigms, engineers are equipped to design robust, low-latency communication infrastructures that drive advanced cyber-physical deployments and mission-critical industrial applications.

Course Objectives

1. To analyze the deterministic requirements and architectural frameworks of real-time communication systems in distributed embedded environments.
2. To evaluate the performance characteristics of various wired and wireless real-time protocols under strict timing constraints.
3. To design robust communication interfaces and network topologies tailored for mission-critical industrial and cyber-physical applications.

Unit I: Fundamentals of Real-Time Communication **9 Hours**
Real-time system constraints - Deterministic network modeling - Message scheduling algorithms - Clock synchronization techniques - Traffic shaping mechanisms - Latency and jitter analysis - Reliability in time-critical networks - Real-time communication architectures - Quality of service provisioning.
Active Learning Activity: Flipped classroom discussion on the comparative analysis of message scheduling algorithms followed by a deterministic network modeling exercise.

Unit II: Fieldbus and Industrial Protocols **9 Hours**
Controller area network architectures - Local interconnect network fundamentals - Flexible data-rate protocol extensions - Time-triggered protocol integration - Media access control strategies - Process fieldbus communication - Advanced telemetry protocols - Multi-master bus arbitration - Legacy interface adaptations.
Active Learning Activity: Simulation-based laboratory utilizing a general network simulator to evaluate latency and collision avoidance in multi-master bus arbitration setups.

Unit III: Real-Time Ethernet Technologies **9 Hours**
Standard Ethernet limitations - Time-sensitive networking fundamentals - Precision time protocol mechanisms - Deterministic switching architectures - Preemption and traffic scheduling - Redundancy in industrial networks - EtherCAT operational principles - PROFINET real-time implementation - Network topology optimization.
Active Learning Activity: Group project designing a deterministic switching architecture using an architecture simulator to measure timing precision across synchronized nodes.

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Unit IV: Wireless Real-Time Protocols **9 Hours**

Wireless real-time challenges - Deterministic wireless communication standards - Time-slotted channel hopping - Wireless sensor network routing - Industrial wireless local area networks - Low-power wide-area network timing - Interference mitigation techniques - Reliable data delivery models - Wireless mesh network synchronization.

Active Learning Activity: Case study analysis of interference mitigation in industrial wireless local area networks followed by an interactive reliable data delivery modeling session.

Unit V: Performance Evaluation and System Design **9 Hours**

Network performance metrics - Protocol conformance testing - Hardware-software co-design interfaces - Embedded network stack optimization - Security in real-time protocols - Fault-tolerant communication design - Cyber-physical system integration - Scalability in distributed networks - Next-generation communication trends.

Active Learning Activity: Design thinking workshop to architect a fault-tolerant communication topology incorporating hardware-software co-design interfaces for a distributed cyber-physical system.

Course Outcomes (COs)

CO1: Analyze the fundamental constraints, scheduling algorithms, and synchronization techniques critical to real-time communication systems. (K4)

CO2: Evaluate the architectural nuances and performance metrics of advanced fieldbus and industrial communication protocols. (K4)

CO3: Apply time-sensitive networking principles and deterministic Ethernet standards to optimize latency in industrial environments. (K3)

CO4: Analyze the challenges and deterministic methodologies associated with implementing wireless real-time communication standards. (K4)

CO5: Design and evaluate secure, fault-tolerant communication architectures for complex distributed cyber-physical systems. (K4)

Resources

1. Reference Books

1. Kopetz, H. (2019). Real-Time Systems: Design Principles for Distributed Embedded Applications. Springer.
2. Seiger, R., & Kumar, A. (2022). Industrial Communication Technology Handbook. CRC Press.
3. Rostami, A. (2021). Time-Sensitive Networks: A Comprehensive Guide. Wiley.
4. Wang, L. (2020). Wireless Real-Time Communication Networks. Artech House.
5. Ergen, M. (2023). Deterministic Communication in Cyber-Physical Systems. IEEE Press.

2. E-Resources

1. IEEE Communications Society Resource Center
   `https://www.comsoc.org/resources`

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2. Time-Sensitive Networking Task Group Documentation
   `https://1.ieee802.org/tsn/`
3. Controller Area Network in Automation (CiA) Specifications
   `https://www.can-cia.org/standardization/`
4. Industrial Ethernet Book Digital Archive
   `https://iebmedia.com/`
5. PROFINET System Description and Technical Guidelines
   `https://www.profibus.com/technology/profinet`

3. Advanced Readings

1. IEEE Standards Association. (2023). Standard for Local and Metropolitan Area Networks: Timing and Synchronization.
2. Association for Computing Machinery. (2024). ACM Transactions on Embedded Computing Systems.
3. International Electrotechnical Commission. (2022). Industrial Communication Networks Profiles.
4. National Institute of Standards and Technology. (2021). Guidelines for Real-Time Wireless Network Deployments.
5. Journal of Real-Time Image Processing and Communications. (2025). Special Issue on Deterministic Networks.

Industrial Relevance

This course is structurally aligned with the escalating global demand for high-speed, deterministic data exchange within modern semiconductor and embedded engineering sectors. As industries transition towards fully integrated cyber-physical systems, autonomous robotics, and time-critical smart infrastructure, the necessity for robust real-time communication networks becomes paramount. By mastering both legacy fieldbus adaptations and next-generation time-sensitive networking standards, graduates are prepared to seamlessly bridge the gap between embedded hardware and reliable distributed control systems. This expertise directly addresses current industrial imperatives for secure, low-latency, and fault-tolerant communication backbones essential for next-generation automated deployments.

CO-PO Articulation Matrix

Course Outcomes	PO1	PO2	PO3
CO1	3	2	3
CO2	2	1	3
CO3	3	2	3
CO4	2	1	3
CO5	3	3	3
Weighted Average	2.60	1.80	3.00

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Course Code: P25VEE65
Course Title: Embedded Systems Security
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4,9,16

Course Overview

This course provides a comprehensive exploration of security methodologies for modern embedded systems, focusing on mitigating hardware and software vulnerabilities in resource-constrained environments. It delves into the integration of cryptographic protocols, secure boot architectures, and trusted execution environments essential for robust electronic system design. By bridging foundational security principles with advanced threat modeling, the curriculum prepares engineers to develop resilient embedded solutions for automotive, industrial, and edge-computing applications.

Course Objectives

1. Formulate comprehensive threat models and risk assessment strategies to identify and mitigate vulnerabilities across hardware and software boundaries in embedded architectures.
2. Integrate cryptographic algorithms and trusted execution environments into embedded platforms to ensure data confidentiality, operational integrity, and robust system authentication.
3. Architect resilient, compliance-driven embedded solutions utilizing industry security frameworks to counteract emerging cyber-physical threats in automation and vehicular networks.

Unit I: Fundamentals of Embedded Systems Security **9 Hours**
Security principles - threat modeling techniques - attack surface analysis - hardware vulnerability assessment - software exploitation methods - secure system architecture - risk evaluation metrics - security lifecycle management - industry compliance standards.
Active Learning Activity: Group-based threat modeling exercise evaluating a generic smart home architecture to map potential attack vectors and formulate preliminary hardware mitigation strategies.

Unit II: Cryptography and Secure Communication **9 Hours**
Symmetric encryption mechanisms - asymmetric cryptographic algorithms - cryptographic hash functions - digital signature generation - key lifecycle management - transport layer security protocols - secure communication frameworks - public key infrastructure - lightweight authentication schemes.
Active Learning Activity: Mathematical problem-solving session focusing on calculating the computational overhead and power consumption metrics of symmetric cryptographic algorithms deployed on resource-constrained microcontrollers.

Unit III: Hardware-Assisted Security **9 Hours**
Secure boot sequence - hardware root of trust - trusted platform modules - trusted execution environments - secure instruction set extensions - physical unclonable functions - hardware

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security modules - secure firmware update mechanisms - cryptographic accelerators.
Active Learning Activity: Architecture analysis task designing a state machine representing a secure boot flow for a generic embedded processor to validate cryptographic firmware signatures.

Unit IV: Secure Embedded Platforms **9 Hours**
Embedded operating system security - real-time task isolation - connected device vulnerabilities - automotive cybersecurity frameworks - industrial control system protection - over-the-air update security - side-channel vulnerability analysis - fault injection mitigation - privilege escalation prevention.
Active Learning Activity: System design simulation isolating critical control routines from non-secure secondary applications using a generic virtualization hypervisor approach.

Unit V: Emerging Trends in Embedded Security **9 Hours**
Secure edge artificial intelligence - machine learning assisted threat detection - secure chiplet integrations - zero trust architecture principles - lightweight cryptographic standards - post-quantum cryptographic concepts - security certification pathways - hardware supply chain security - future embedded threat landscapes.
Active Learning Activity: Research case study analysis evaluating the latency and performance impact of transitioning legacy industrial embedded systems to strict zero trust network principles.

Course Outcomes (COs)

1. CO1: Analyze hardware and software vulnerabilities to construct comprehensive threat models for modern embedded systems. (K4)
2. CO2: Select and implement appropriate cryptographic algorithms and secure communication protocols for resource-constrained platforms. (K3)
3. CO3: Examine trusted execution environments and hardware root of trust mechanisms to validate platform integrity. (K4)
4. CO4: Analyze industry-specific security frameworks to evaluate protective measures for automotive and industrial embedded applications. (K4)
5. CO5: Architect comprehensive security strategies integrating advanced hardware mitigation techniques to protect emerging cyber-physical systems. (K4)

Resources

1. Reference Books

1. Stallings, W. (2020). Cryptography and network security: Principles and practice (8th ed.). Pearson.
2. Anderson, R. J. (2020). Security engineering: A guide to building dependable distributed systems (3rd ed.). Wiley.
3. John, L. K., & John, E. (2020). Hardware security and trust: Design and deployment of integrated circuits in a threatened environment. Springer.
4. Tehranipoor, F. (2021). Hardware security: A hands-on learning approach. Elsevier.
5. Ali, A. M. H. (2022). IoT security: Advances in authentication. Wiley.

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2. E-Resources

1. National Institute of Standards and Technology. (n.d.). Lightweight Cryptography Project.
   `https://csrc.nist.gov/projects/lightweight-cryptography`
2. Arm Developer. (n.d.). Architecture Security Enhancements Documentation.
   `https://developer.arm.com/architectures/security-features`
3. Open Web Application Security Project. (n.d.). Internet of Things Project.
   `https://owasp.org/www-project-internet-of-things/`
4. International Organization for Standardization. (n.d.). Road Vehicles Cybersecurity Engineering Overview.
   `https://www.iso.org/standard/70918.html`
5. Trusted Computing Group. (n.d.). TPM Library Specifications.
   `https://trustedcomputinggroup.org/work-groups/trusted-platform-module/`

Industrial Relevance

This course is fundamentally aligned with the stringent security demands of the contemporary semiconductor and embedded systems industry, acting as a critical bridge between theoretical cryptographic concepts and practical hardware deployment. As the proliferation of connected devices in automotive, industrial automation, and smart infrastructure expands, vulnerabilities at the hardware-software interface present significant operational risks. By mastering root of trust establishment, secure boot implementation, and side-channel attack mitigation, graduates are directly prepared to meet international compliance mandates. This comprehensive skill set empowers engineers to seamlessly transition into roles involving secure system-on-chip design and resilient architecture development, addressing the global industry's urgent need for secure-by-design cyber-physical systems.

CO-PO Articulation Matrix

Course Outcomes	PO1	PO2	PO3
CO1	3	2	3
CO2	2	1	3
CO3	3	2	3
CO4	3	2	3
CO5	3	3	3
Weighted Average	2.80	2.00	3.00

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MANDATORY COURSES

Course Code: P25VEM01
Course Title: Research Methodology and Intellectual Property Rights
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
SDG: 4, 8, 9

Course Overview

This course provides a rigorous foundation in engineering research methodologies, equipping students with the analytical skills necessary for advanced scientific inquiry in VLSI and embedded systems. It explores the comprehensive lifecycle of technical research, encompassing literature evaluation, experimental design, statistical validation, and professional scientific communication. Furthermore, the curriculum integrates essential knowledge of Intellectual Property Rights (IPR) and patent strategies, ensuring graduates can effectively protect and commercialize hardware innovations within the global semiconductor ecosystem.

Course Objectives

1. Formulate robust engineering research problems and hypotheses tailored to semiconductor and embedded system domains using systematic inquiry techniques.
2. Design rigorous experimental frameworks and apply statistical data analysis methodologies to validate hardware and software architectural solutions.
3. Develop comprehensive technical publications and patent disclosures that adhere to professional ethical standards and intellectual property regulations.

Unit I: Engineering Research Methodology **9 Hours**
Research objectives and engineering scope - Quantitative and qualitative research types - Algorithmic and hardware research processes - Technical problem identification techniques - Systematic research gap analysis - Falsifiable hypothesis formulation - Empirical research design strategies - Responsible conduct of engineering research - Ethical standards in semiconductor studies.
Active Learning Activity: Group-based research problem formulation exercise utilizing current semiconductor industry white papers to identify and present specific technological gaps.

Unit II: Literature Survey and Scientific Communication **9 Hours**
Scientific literature repository navigation - Advanced search string construction - Systematic literature review methodologies - Citation metrics and impact factors - Automated reference management workflows - Technical report structuring - Hardware specification documentation - Scholarly engineering presentations - Peer-review response formulation.
Active Learning Activity: Hands-on literature mapping session using general-purpose scholarly databases to construct a visual citation network for a specific VLSI domain.

Unit III: Experimental Design and Data Analysis **9 Hours**
Hardware experimental planning - Quantitative data collection methods - Fractional factorial design of experiments - Statistical significance testing - Linear and non-linear regression models - Multivariate correlation analysis - Multi-dimensional data visualization - Empirical result interpretation - Reproducible validation practices.

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Active Learning Activity: Simulation-based statistical analysis utilizing general-purpose numerical computing environments to evaluate correlation matrices of power and performance metrics.

Unit IV: Intellectual Property Rights **9 Hours**
Fundamentals of intellectual property frameworks - Hardware utility patents - Software and firmware copyrights - Semiconductor industry trademarks - Integrated circuit layout-design protection - Geographical indications for technology hubs - Patent search and prior art analysis - Technical patent drafting strategies - Technology licensing and commercialization protocols.
Active Learning Activity: Interactive patent landscaping workshop analyzing open-access patent databases to map the intellectual property history of an emerging microarchitecture.

Unit V: Research Publication, Innovation and Entrepreneurship **9 Hours**
Grant and research proposal preparation - High-impact journal formatting constraints - Conference publication paradigms - Rigorous peer-review mechanics - Publication ethics and integrity - Predatory publishing identification - Advanced plagiarism detection mechanisms - Technology innovation management - Hardware startup ecosystem and entrepreneurship.
Active Learning Activity: Role-play peer-review committee session evaluating anonymized excerpts of hardware research proposals against standardized academic criteria.

Course Outcomes

1. CO1: Formulate systematic engineering research problems and falsifiable hypotheses for advanced hardware systems. (K4)
2. CO2: Analyze academic literature using scholarly databases to identify empirical gaps in existing semiconductor technologies. (K4)
3. CO3: Apply experimental design frameworks and statistical evaluation methods to validate engineering methodologies. (K3)
4. CO4: Examine intellectual property rights, patent architectures, and layout-design protections relevant to the technology sector. (K4)
5. CO5: Construct comprehensive research proposals, technical publications, and patent disclosures aligned with industry standards. (K3)

Resources

1. Reference Books

1. Creswell, J. W., & Creswell, J. D. (2022). Research design: Qualitative, quantitative, and mixed methods approaches (6th ed.). SAGE Publications.
2. Thiel, D. V. (2023). Research methods for engineers (2nd ed.). Cambridge University Press.
3. Leedy, P. D., & Ormrod, J. E. (2024). Practical research: Planning and design (13th ed.). Pearson.
4. Stim, R. (2022). Patent, copyright & trademark: An intellectual property desk reference (17th ed.). Nolo.
5. Day, R. A., & Gastel, B. (2024). How to write and publish a scientific paper (9th ed.). Cambridge University Press.

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2. E-Resources

1. World Intellectual Property Organization (WIPO) Academy
   `https://welc.wipo.int/`
2. IEEE Intellectual Property Rights Guidelines
   `https://www.ieee.org/publications/rights/`
3. National Institutes of Health (NIH) Data Management and Sharing Policy
   `https://sharing.nih.gov/`
4. United States Patent and Trademark Office (USPTO) Patent Search Portal
   `https://ppubs.uspto.gov/pubwebapp/`
5. MIT OpenCourseWare: Patents, Copyrights, and the Law of Intellectual Property
   `https://ocw.mit.edu/courses/15-564-patents-copyrights-and-the-law-of-intellectual-prop`

3. Text Books

1. Kothari, C. R., & Garg, G. (2019). Research methodology: Methods and techniques (4th ed.). New Age International.
2. Kumar, R. (2019). Research methodology: A step-by-step guide for beginners (5th ed.). Sage Publications.
3. Gopalakrishnan, N. S., & Agitha, T. G. (2020). Principles of intellectual property (3rd ed.). Eastern Book Company.

Industrial Relevance

The integration of sophisticated research methodologies and intellectual property frameworks is a cornerstone of modern semiconductor and embedded systems engineering. In the highly competitive global hardware industry, the ability to rapidly prototype, empirically validate, and rigorously document novel microarchitectures directly correlates with time-to-market and technological leadership. By mastering the processes of scientific inquiry, engineers can systematically eliminate design flaws, while expertise in intellectual property rights ensures that costly research and development investments are legally protected against infringement. This comprehensive understanding enables professionals to seamlessly transition from academic research environments into leading-edge industrial research laboratories, empowering them to drive semiconductor innovation, navigate complex patent landscapes, and commercialize next-generation embedded technologies effectively.

CO-PO Articulation Matrix

Course Outcomes	PO1	PO2	PO3
CO1	3	1	2
CO2	3	2	2
CO3	3	2	3
CO4	1	1	2
CO5	2	3	2
Weighted Average	2.40	1.80	2.20

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