SEMESTER I

S.No	Course Code	Course Title	CC	L	T	P	C	CP	SDG
1	P25MTA02	Mathematical Foundations for VLSI and Embedded Systems	FC	3	1	0	4	4	4
2	P25VET01	Advanced Digital CMOS IC Design	PC	3	0	0	3	3	4,9
3	P25VET02	Analog and Mixed-Signal IC Design	PC	3	0	0	3	3	4,9
4	P25VET03	Embedded Systems Design and Applications	PC	3	0	0	3	3	4,9
5	P25VET04	Embedded Processor Architectures	PC	3	0	0	3	3	4,9
6	P25VEM01	Research Methodology and Intellectual Property Rights	MC	3	0	0	3	3	4,9,8
7	P25VEP01	Advanced Embedded Systems Laboratory	PC	0	0	4	2	4	4,9
8	-	Bridge Course #	BC	2	0	0	0	2	*
			Total	**20**	**1**	**4**	**21**	**25**	

SEMESTER II

S.No	Course Code	Course Title	CC	L	T	P	C	CP	SDG
1	P25VET05	Advanced SoC Architecture	PC	3	0	0	3	3	4,9
2	P25VET06	Physical Design and Signoff	PC	3	0	0	3	3	4,9
3	P25VET07	Real-Time Operating Systems	PC	3	0	0	3	3	4,9
4	P25VET08	AI for VLSI and Embedded Systems	PC	3	0	0	3	3	4,9
5	P25VEEXX	Professional Elective I	PE	3	0	0	3	3	*
6	P25VEP02	Advanced SoC Design Laboratory	PC	0	0	4	2	4	4,9
7	P25VEI01	Industrial Training	IOC	0	0	0	1	-	4,8,9
8	-	Self-Learning Course	SLC	0	0	0	1	-	*
			Total	**15**	**0**	**4**	**19**	**19**	

SEMESTER III

S.No	Course Code	Course Title	CC	L	T	P	C	CP	SDG
1	P25VEEXX	Professional Elective II	PE	3	0	0	3	3	*
2	P25VEEXX	Professional Elective III	PE	3	0	0	3	3	*
3	P25VEEXX	Professional Elective IV	PE	3	0	0	3	3	*
4	P25VEEXX	Professional Elective V	EEC	3	0	0	3	3	*
5	P25VEJ01	Project Work Phase I	EEC	0	0	16	8	16	*
			Total	**12**	**0**	**16**	**20**	**28**	

SEMESTER IV

S.No	Course Code	Course Title	CC	L	T	P	C	CP	SDG
1	P25VEJ02	Project Work Phase II	EEC	0	0	24	12	24	*
			Total	**0**	**0**	**24**	**72**	**31**	

*SDG mapping shall depend on the course selected.
#Note: Applicable only to students from allied disciplines as determined by the Department.