CIET COIMBATORE INSTITUTE OF ENGINEERING AND TECHNOLOGY

CURRICULUM & SYLLABUS

R 2023

(Choice Based Credit System)

B.E. Electronics Engineering (VLSI Design & Technology)

www.cietcbe.edu.in/eevlsi

Department of Electronics Engineering

About the Department

The Department of Electronics Engineering, established in 2024, offers the B.E. Electronics Engineering (VLSI Design and Technology) programme with an annual intake of 30 students and the M.E. VLSI Design and Embedded Systems programme with an annual intake of 6 students. The department provides a strong foundation and advanced learning in electronics, signal and image processing, VLSI design, semiconductor technologies, and embedded systems. The curriculum is periodically reviewed and updated to keep pace with technological advancements, industry requirements, and societal needs. The department promotes practical learning, research, innovation, and continuous academic development to prepare graduates for successful careers in industry, research, higher education, and entrepreneurship.

Vision

To develop competent engineering professionals with strong knowledge and practical skills in VLSI and emerging technologies, fostering research, innovation, and ethical values to meet the needs of industry and society.

Mission

MS1: Technical Knowledge and Innovation: To provide quality education in VLSI and emerging technologies through effective teaching, continuous learning, research, and innovation.
MS2: Practical Skills and Industry Exposure: To develop practical and professional skills through laboratory learning, projects, internships, industrial training, and interaction with industry.
MS3: Professional and Ethical Development: To develop communication, leadership, entrepreneurial, and lifelong learning skills while promoting professional ethics and social responsibility.

Program Educational Objectives (PEO)

PEO 1 : Employment: Graduates will establish successful careers in the semiconductor and related industries by applying strong technical knowledge and practical skills in VLSI and emerging technologies.
PEO 2 : Enhancement: Graduates will enhance their professional competence through higher education, continuous learning, and the application of advanced VLSI design methodologies and emerging technologies.
PEO 3 : Advancement: Graduates will advance professionally through innovation, entrepreneurship, leadership, and ethical practices while contributing to technological and societal development.

Program Specific Outcomes (PSO)

PSO 1 : Develop problem-solving skills in VLSI design and technology through understanding fundamental concepts of Electronics, Signal, Image Processing, Communication and Embedded

Systems utilizing EDA (Electronic Design Automation tools), designing complex circuits, and optimizing circuit performance.
PSO 2 : Acquire professional skills in VLSI design and technology by gaining knowledge of fabrication processes, exploring advanced topics like ASIC design and FPGA implementation, and applying industry-standard design methodologies.
PSO 3 : Prepare students for successful careers and entrepreneurship in VLSI design and technology by equipping them with problem-solving abilities, industry-relevant skills, and the capability to apply Semiconductor Physics, Computer Science, Electrical, Electronics, Communication, VLSI knowledge in Industries and entrepreneurial ventures.

Knowledge and Attitude Profile (WK)

WK1: A systematic, theory-based understanding of the natural sciences applicable to the discipline and awareness of relevant social sciences.
WK2: Conceptually-based mathematics, numerical analysis, data analysis, statistics and formal aspects of computer and information science to support detailed analysis and modelling applicable to the discipline.
WK3: A systematic, theory-based formulation of engineering fundamentals required in the engineering discipline.
WK4: Engineering specialist knowledge that provides theoretical frameworks and bodies of knowledge for the accepted practice areas in the engineering discipline; much is at the forefront of the discipline.
WK5: Knowledge, including efficient resource use, environmental impacts, whole-life cost, reuse of resources, net zero carbon, and similar concepts, that supports engineering design and operations in a practice area.
WK6: Knowledge of engineering practice (technology) in the practice areas in the engineering discipline.
WK7: Knowledge of the role of engineering in society and identified issues in engineering practice in the discipline, such as the professional responsibility of an engineer to public safety and sustainable development.
WK8: Engagement with selected knowledge in the current research literature of the discipline, awareness of the power of critical thinking and creative approaches to evaluate emerging issues.
WK9: Ethics, inclusive behavior and conduct. Knowledge of professional ethics, responsibilities, and norms of engineering practice. Awareness of the need for diversity by reason of ethnicity, gender, age, physical ability etc. with mutual understanding and respect, and of inclusive attitudes.

Program Outcomes (PO)

PO 1 – Engineering Knowledge: Apply knowledge of mathematics, natural science, computing, engineering fundamentals and an engineering specialization as specified in WK1 to WK4 respectively to develop solutions to complex engineering problems.

PO 2 – Problem Analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions with consideration for sustainable development.

PO 3 – Design/Development of Solutions: Design creative solutions for complex engineering problems and design/develop systems/components/processes to meet identified needs with consideration for public health and safety, whole-life cost, net zero carbon, culture, society and environment as required.

PO 4 – Conduct Investigations of Complex Problems: Conduct investigations of complex engineering problems using research-based knowledge including design of experiments, modelling, analysis and interpretation of data to provide valid conclusions.

PO 5 – Engineering Tool Usage: Create, select and apply appropriate techniques, resources and modern engineering and IT tools, including prediction and modelling, recognizing their limitations to solve complex engineering problems.

PO 6 – The Engineer and the World: Analyze and evaluate societal and environmental aspects while solving complex engineering problems for their impact on sustainability with reference to economy, health, safety, legal framework, culture and environment.

PO 7 – Ethics: Apply ethical principles and commit to professional ethics, human values, diversity and inclusion; adhere to national and international laws.

PO 8 – Individual and Collaborative Teamwork: Function effectively as an individual, and as a member or leader in diverse/multidisciplinary teams.

PO 9 – Communication: Communicate effectively and inclusively within the engineering community and society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations considering cultural, language and learning differences.

PO 10 – Project Management and Finance: Apply knowledge and understanding of engineering management principles and economic decision-making and apply these to one's own work, as a member and leader in a team, and to manage projects and in multidisciplinary environments.

PO 11 – Life-Long Learning: Recognize the need for, and have the preparation and ability for: (i) independent and life-long learning, (ii) adaptability to new and emerging technologies, and (iii) critical thinking in the broadest context of technological change.

Sustainable Development Goals (SDG)

SDG	**Sustainable Development Goal**
SDG 1	No Poverty
SDG 2	Zero Hunger
SDG 3	Good Health and Well-being
SDG 4	Quality Education
SDG 5	Gender Equality
SDG 6	Clean Water and Sanitation
SDG 7	Affordable and Clean Energy
SDG 8	Decent Work and Economic Growth
SDG 9	Industry, Innovation and Infrastructure
SDG 10	Reduced Inequalities
SDG 11	Sustainable Cities and Communities
SDG 12	Responsible Consumption and Production
SDG 13	Climate Action
SDG 14	Life Below Water
SDG 15	Life on Land
SDG 16	Peace, Justice and Strong Institutions
SDG 17	Partnerships for the Goals

SEMESTER I

S.No	Course Code	Course Title	CC	L	T	P	C	CP	SDG
Induction Programme									
1	U23MTA01	Induction Programme	MT	0	0	0	0	0	3,4,5,10,16
Theory									
2	U23MAT01	Linear Algebra and Calculus	BS	3	1	0	4	4	4,9
3	U23EGT01	Communicative English	HS	3	0	0	3	3	4
4	U23PYT01	Engineering Physics	BS	3	0	0	3	3	4,7,9
5	U23CST01	Problem Solving and Programming in C	ES	3	0	0	3	3	4,9
6	U23TAT01	Heritage of Tamils	HS	1	0	0	1	1	4,11
Practical's									
7	U23PYP01	Physics Laboratory	BS	0	0	2	1	2	4,9
8	U23CSP01	Problem Solving and Programming in C Laboratory	ES	0	0	2	1	2	4,9
9	U23MEP02	Engineering Drawing	ES	0	0	4	2	4	4,9
			Total	**13**	**1**	**8**	**18**	**22**	

SEMESTER II

S.No	Course Code	Course Title	CC	L	T	P	C	CP	SDG
Theory									
1	U23MAT02	Transforms and Boundary value problems	BS	3	1	0	4	3	4,9
2	U23CYT01	Engineering Chemistry	BS	3	0	0	3	4	6,7,12
3	U23CST02	Python Programming	ES	3	0	0	3	3	4,9
4	U23ECT01	Electric Circuit and Electron Devices	PC	3	0	0	3	3	7,9
5	U23EGT02	Professional English	HS	3	0	0	3	3	4,8
6	U23TAT02	Tamils and Technology	HS	1	0	0	1	1	4,9,11
Practical's									
7	U23CYP01	Chemistry Laboratory	BS	0	0	2	1	2	6,12
8	U23CSP02	Python Programming Laboratory	ES	0	0	2	1	2	4,9
9	U23ECP04	Electric Circuit and Electron Devices Laboratory	PC	0	0	2	1	2	7,9
			Total	**16**	**1**	**6**	**20**	**23**	

SEMESTER III

S.No	Course Code	Course Title	CC	L	T	P	C	CP	SDG
Theory									
1	U23MAT06	Probability and Random Process	BS	3	1	0	4	4	4&9
2	U23CST03	Data Structures	ES	3	0	0	3	3	4&9
3	U23EVT31	Digital System Design	PC	3	0	0	3	3	9
4	U23EVT01	Analog and Digital Communication	PC	3	0	0	3	3	9,11
5	U23EVT02	Electronic Devices and Circuits	PC	3	0	0	3	3	7,9
Practical's									
6	U23CSP03	Data Structures Laboratory	ES	0	0	2	2	4	4,9
7	U23EVP31	Digital System Design Laboratory	PC	0	0	4	2	4	9
8	U23EVP01	Analog and Digital Communication Lab	PC	0	0	2	2	4	9,11
9	U23EVP02	Electronic Devices and Circuits Laboratory	PC	0	0	2	2	4	7,9
10	U23EVI01	Core Course Project I	EEC	0	0	2	1	2	4,9
			Total	**15**	**1**	**12**	**25**	**34**	

SEMESTER IV

S.No	Course Code	Course Title	CC	L	T	P	C	CP	SDG
Theory									
1	U23ECT10	Linear Integrated Circuits	PC	3	0	0	3	3	7,9
2	U23EVT03	Electro Magnetic Fields and Transmission lines	PC	3	0	0	3	3	7,9
3	U23EVT04	SystemVerilog	PC	3	0	0	3	3	4,9
4	U23EVT05	Analog Integrated Circuits Design	PC	3	0	0	3	3	7,9
5	U23EVT06	CMOS Integrated Circuits	PC	3	0	0	3	3	7,9,12
6	U23XXXXX	Mandatory Course I	MT	2	0	0	0	2	***
Practical's									
7	U23ECP10	Linear Integrated Circuits Laboratory	PC	0	0	4	2	4	7,9
8	U23EVP03	Hardware modelling Using SystemVerilog Laboratory	PC	0	0	4	2	4	4,9
9	U23EVP04	CMOS IC Laboratory	PC	0	0	4	2	4	7,9,12
10	U23EVI02	Core Course Project II	EEC	0	0	4	1	2	4,9
			Total	**17**	**0**	**16**	**22**	**31**	

SEMESTER V

S.No	Course Code	Course Title	CC	L	T	P	C	CP	SDG
Theory									
1	U23EVT07	Digital Signal Processing Algorithms	PC	3	0	0	3	3	9
2	U23EVT08	Computer Architecture and On-Chip Communication	PC	3	0	3	3	3	9
3	U23EVT09	Semiconductor Manufacturing Technology	PC	3	0	0	3	3	7,9,12
4	U23EVT10	SoC Design I: RTL Design and Verification	PC	3	0	0	3	3	9
5	U23EXXXX	Professional Elective - I	PE	3	0	0	3	3	*
6	U23XXXX	Open Elective - I	OE	3	0	0	3	3	**
7	U23XXXXX	Mandatory Course II	MT	2	0	0	0	2	***
Practical's									
8	U23EVP05	Digital Signal Processing Laboratory	PC	0	0	2	2	4	9
9	U23EVP06	RTL Design and Verification Laboratory	PC	0	0	2	2	4	9
10	U23EVI03	Core Course Project III	EEC	0	0	4	1	2	4,9
			Total	**20**	**0**	**11**	**22**	**30**	

SEMESTER VI

S.No	Course Code	Course Title	CC	L	T	P	C	CP	SDG
Theory									
1	U23EVT11	Embedded Systems Architecture and Design	PC	3	0	0	3	3	7,9,11
2	U23EVT12	VLSI Testing and Validation	PC	3	0	0	3	3	9,12
3	U23EVT13	SoC Design II: Physical Design and Chip Implementation	PC	3	0	0	3	3	7,9,12
4	U23EVT14	Wireless Communication Systems	PC	3	0	0	3	3	9,11
5	U23EXXXX	Professional Elective - II	PE	3	0	0	3	3	*
6	U23XXXX	Open Elective - II	OE	3	0	0	3	3	**
Practical's									
7	U23EVP07	Embedded Systems Laboratory	PC	0	0	2	2	4	9,11
8	U23EVP08	Physical Design Laboratory	PC	0	0	2	2	4	7,9,12
9	U23EVI04	Core Course Project IV	EEC	0	0	4	1	2	4,9
			Total	**18**	**0**	**8**	**23**	**28**	

SEMESTER VII									
S.No	**Course Code**	**Course Title**	**CC**	**L**	**T**	**P**	**C**	**CP**	**SDG**
Theory									
1	U23EVT15	Electronic Packaging and PCB Design	PC	3	0	0	3	3	9,12
2	U23EXXXX	Professional Elective - III	PE	3	0	0	3	3	*
3	U23EXXXX	Professional Elective - IV	PE	3	0	0	3	3	*
4	U23EXXXX	Professional Elective - V	PE	3	0	0	3	3	*
5	U23EXXXX	Professional Elective - VI	PE	3	0	0	3	3	*
Practical's									
6	U23EVP09	Electronic Packaging and PCB Prototyping Laboratory	PC	0	0	2	2	4	9,12
7	U23EVJ01	Project Work Phase I	EEC	0	0	12	6	12	8,9,12
			Total	**12**	**0**	**14**	**23**	**31**	

SEMESTER VIII									
S.No	**Course Code**	**Course Title**	**CC**	**L**	**T**	**P**	**C**	**CP**	**SDG**
1	U23EVJ02	Project Work Phase II / Internship	EEC	0	0	12	12	12	8,9,12,17
			TOTAL CREDITS				**167**		

Vertical I – Advanced Digital Design, Verification and FPGA Systems									
S.No	**Course Code**	**Course Title**	**CC**	**L**	**T**	**P**	**C**	**CP**	**SDG**
1	U23EVV51	FPGA Design and Implementation	PE	3	0	0	3	3	4,9
2	U23EVV52	High-Level Synthesis for FPGA and ASIC	PE	3	0	0	3	3	7,9,12
3	U23EVV53	Universal Verification Methodology	PE	3	0	0	3	3	4,9
4	U23EVV54	Semiconductor Memory Technologies	PE	3	0	0	3	3	7,9,12
5	U23EVV55	Hardware Security and Trust	PE	3	0	0	3	3	9,16
6	U23EVV56	EDA Scripting and Semiconductor Design Automation	PE	3	0	0	3	3	4,9

Vertical II – Embedded Vision and Intelligent Image Processing Systems									
S.No	**Course Code**	**Course Title**	**CC**	**L**	**T**	**P**	**C**	**CP**	**SDG**
1	U23EVV57	Digital Image Processing	PE	3	0	0	3	3	3,9
2	U23EVV58	Computer Vision for Embedded Systems	PE	3	0	0	3	3	3,9,11
3	U23EVV59	FPGA-Based Image and Video Processing	PE	3	0	0	3	3	9
4	U23EVV60	CMOS Image Sensors and Camera Systems	PE	3	0	0	3	3	3,9,11
5	U23EVV61	AI Accelerators for Vision Systems	PE	3	0	0	3	3	7,9
6	U23EVV62	Edge AI Vision Systems	PE	3	0	0	3	3	7,9,11

Vertical III – Semiconductor Manufacturing, Reliability and Product Engineering									
S.No	**Course Code**	**Course Title**	**CC**	**L**	**T**	**P**	**C**	**CP**	**SDG**
1	U23EVV63	Semiconductor Process Integration	PE	3	0	0	3	3	9,12
2	U23EVV64	Advanced Lithography and Process Technologies	PE	3	0	0	3	3	9,12
3	U23EVV65	Semiconductor Device Modeling using TCAD	PE	3	0	0	3	3	7,9
4	U23EVV66	Semiconductor Reliability and Yield Engineering	PE	3	0	0	3	3	9,12
5	U23EVV67	Advanced Semiconductor Packaging	PE	3	0	0	3	3	9,12
6	U23EVV68	Semiconductor Product Engineering and Failure Analysis	PE	3	0	0	3	3	9,12

Vertical IV – Embedded Systems, IoT and Edge Computing									
S.No	**Course Code**	**Course Title**	**CC**	**L**	**T**	**P**	**C**	**CP**	**SDG**
1	U23EVV69	Real-Time Embedded Software and Systems	PE	3	0	0	3	3	9,11
2	U23EVV70	Embedded Linux and Device Drivers	PE	3	0	0	3	3	4,9
3	U23EVV71	Embedded Communication Protocols	PE	3	0	0	3	3	9,11
4	U23EVV72	Internet of Things System Design	PE	3	0	0	3	3	7,9,11
5	U23EVV73	Edge Computing Systems	PE	3	0	0	3	3	7,9,11
6	U23EVV74	Embedded AI and TinyML	PE	3	0	0	3	3	7,9,11

Vertical V – Analog, Mixed-Signal and RF Integrated Circuit Design									
S.No	**Course Code**	**Course Title**	**CC**	**L**	**T**	**P**	**C**	**CP**	**SDG**
1	U23EVV75	Data Converter Design	PE	3	0	0	3	3	7,9
2	U23EVV76	PLL and Clock Generation Circuits	PE	3	0	0	3	3	7,9
3	U23EVV77	Power Management Integrated Circuits	PE	3	0	0	3	3	7,9,12
4	U23EVV78	Advanced Mixed-Signal IC Design	PE	3	0	0	3	3	7,9
5	U23EVV79	RF Integrated Circuit Design	PE	3	0	0	3	3	7,9
6	U23EVV80	Mixed-Signal Verification	PE	3	0	0	3	3	4,9

Vertical VI – Emerging Computing Architectures and Semiconductor Systems									
S.No	**Course Code**	**Course Title**	**CC**	**L**	**T**	**P**	**C**	**CP**	**SDG**
1	U23EVV781	Quantum Computing Architectures and Hardware	PE	3	0	0	3	3	9
2	U23EVV82	Neuromorphic Computing Systems	PE	3	0	0	3	3	7,9
3	U23EVV83	High-Performance Computing Architectures	PE	3	0	0	3	3	9
4	U23EVV84	Photonic Computing and Optical Interconnects	PE	3	0	0	3	3	7,9
5	U23EVV85	Chiplet-Based and Heterogeneous Computing Systems	PE	3	0	0	3	3	9,12
6	U23EVV86	Approximate Computing Architectures	PE	3	0	0	3	3	7,9

*SDG Mapping for Professional Electives shall be based on the specific elective form corresponding to the respective verticals. **SDG Mapping for Open Electives shall depend on the course selected. ***SDG Mapping for Mandatory Courses shall depend on the course selected.

Summary of Credit Distribution											
S.No.	**CAT**	**Credits / Semester**								**Total Credits**	**Percentage of Total Credits**
		I	**II**	**III**	**IV**	**V**	**VI**	**VII**	**VIII**		
1	BS	8	8	4	0	0	0	0	0	20	11.98
2	ES	6	5	5	0	0	0	0	0	16	9.58
3	HS	4	4	0	0	0	0	0	0	8	4.79
4	PC	0	4	15	21	16	16	5	0	77	46.11
5	PE	0	0	0	0	3	3	12	0	18	10.78
6	OE	0	0	0	0	3	3	0	0	6	3.59
7	EEC	0	0	1	1	1	1	6	12	22	13.17
8	MT	#	0	0	#	#	0	0	0	-	-
	TOTAL	**18**	**20**	**25**	**22**	**23**	**23**	**23**	**12**	**167**	**100.00**

BS – Basic Sciences, ES – Engineering Sciences, HS – Humanities Social Sciences and Management, PC - Professional Core, PE - Professional Elective, OE – Open Elective, EEC Employability Enhancement Course, Mandatory Course.

Course Code: U23MAT01
Course Title: Linear Algebra and Calculus
Course Type: Basic Sciences
L T P C: 3 1 0 4
Total Hours: 60
Prerequisites: -
SDG: 4,9
Common to ALL branches

Course Overview

This course establishes a rigorous mathematical foundation in linear algebra, multivariable calculus, and vector analysis essential for advanced engineering problem-solving. Key themes encompass vector spaces, matrix techniques, functions of several variables, vector differentiation and integration, and multiple integrals evaluated across various coordinate systems. The curriculum directly supports VLSI design and technology by providing the mathematical framework required for semiconductor device modeling, electromagnetic field analysis, circuit simulation, and signal processing algorithms.

Course Objectives

To make the students:

1. Acquaint with the knowledge of vector space and its applications.
2. Develop the use of matrix techniques for practical problems.
3. Familiarize with functions of several variables.
4. Understand the concepts of gradient, divergence and curl through vector differentiation and integration.
5. Interpret with mathematical tools needed in evaluating multiple integrals and their applications.

Unit I: LINEAR ALGEBRA **9 Hours**
Vector spaces - Subspaces - Linear combinations and linear system of equations - Linear independence and linear dependence - Bases and dimensions.

Unit II: MATRICES **9 Hours**
Determinant - Cramer's rule - Eigen values and Eigen vectors of a real matrix - Properties - Cayley Hamilton theorem (statement only) - Application - Elastic Membrane.

Unit III: FUNCTIONS OF SEVERAL VARIABLES **9 Hours**
Limits and Continuity (Geometrical interpretations) - Properties of continuous function - Partial derivatives - Total derivatives - Jacobians - Taylor's series for two variables.

Unit IV: VECTOR CALCULUS **9 Hours**
Gradient and directional derivative - Divergence and curl - Irrotational and Solenoidal vector fields - Line integral over a plane curve - Surface integral - Volume integral - Green's and Stoke's theorems.

Unit V: MULTIPLE INTEGRALS **9 Hours**
Double integration (Cartesian coordinates) - Region of integration - Triple integration in Cartesian coordinates - application of triple integrals.

Course Outcomes (COs)

Upon completion of the course, students would be able to:

- **CO1:** Determine the basis and dimension of vector spaces by applying the concepts of vectors and linear algebra. (K3)
- **CO2:** Solve engineering problems using matrices and linear algebra techniques. (K3)
- **CO3:** Use differentiation techniques in solving real time problems. (K3)
- **CO4:** Compute gradient, divergence, and curl of vector fields and evaluate line, surface, and volume integrals using vector calculus. (K3)
- **CO5:** Evaluate areas, surface area and volume using multiple integrals. (K3)

Resources

1. Text Books

1. Stewart, J. (2016). *Calculus: Early transcendentals* (8th ed.). Cengage Learning, New Delhi.
2. Kreyszig, E. (2016). *Advanced Engineering Mathematics* (10th ed.). John Wiley and Sons (Asia) Ltd, Delhi.

2. Reference Books

1. Jain, R. K., & Iyengar, S. R. K. (2021). *Advanced Engineering Mathematics* (6th ed.). Narosa Publications, New Delhi.
2. Pal, S., & Bhunia, S. C. (2018). *Engineering Mathematics* (2nd ed.). Oxford University Press, India.
3. Lay, D. C. (2016). *Linear Algebra and Its Applications* (5th ed.). Pearson Education, New Delhi.

3. E-Resources

1. NPTEL Course: Linear Algebra and Applications (Note: Vector spaces, linear transformations, and matrix equations)
   `https://nptel.ac.in/courses/111101115`
2. NPTEL Course: Advanced Engineering Mathematics (Note: Multivariable calculus, vector differentiation, and integration)
   `https://nptel.ac.in/courses/111108157`
3. NPTEL Course: Mathematics-I (Note: Calculus of several variables and multiple integrals)
   `https://nptel.ac.in/courses/111105122`
4. MIT OpenCourseWare: Multivariable Calculus (Note: Partial derivatives, Jacobians, Green's, and Stokes' theorems)
   `https://ocw.mit.edu/courses/18-02sc-multivariable-calculus-fall-2010/`
5. MIT OpenCourseWare: Linear Algebra (Note: Determinants, eigenvalues, eigenvectors, and dynamic systems)
   `https://ocw.mit.edu/courses/18-06sc-linear-algebra-fall-2011/`

Industrial Relevance

Linear algebra and calculus form the mathematical backbone of modern Electronic Design Automation (EDA) and semiconductor technology. Matrix operations and linear systems are fundamental to circuit simulation algorithms, interconnect modeling, and layout verification tools used in global chip manufacturing. Multivariable and vector calculus enable the rigorous formulation of Maxwell's equations for electromagnetic interference analysis and semiconductor physics equations for transistor device modeling. By mastering these mathematical principles, engineers gain the essential computational skills required to optimize VLSI circuit performance, design complex integrated hardware, and develop advanced chip architectures in the global semiconductor industry.

CO-PO-PSO Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	-	-	-	-	-	-	2	-	2	3	1	2
CO2	3	3	-	-	-	-	-	-	2	-	2	3	2	2
CO3	3	2	1	1	-	-	-	-	2	-	2	2	1	1
CO4	3	3	1	1	-	-	-	-	2	-	2	3	2	2
CO5	3	3	1	1	-	-	-	-	2	-	2	3	1	2
Weighted Average	3.00	3.00	1.00	1.00	-	-	-	-	2.00	-	2.00	2.80	1.40	1.80

Course Code: U23EGT01
Course Title: Communicative English
Course Type: Humanities and Social Sciences
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: -
SDG: 4,8,9

Course Overview

This course provides undergraduate engineering students with robust English language acquisition and communication methodologies essential for academic and professional success. Key themes encompass technical writing, comprehensive reading strategies, vocabulary enhancement, data interpretation, and business communication protocols. By mastering these communicative competencies, future electronics and VLSI engineers can effectively articulate complex technical concepts, draft industry-standard design documentation, and function collaboratively in global multidisciplinary environments.

Course Objectives

To make the students:

1. Enhance English Language Acquisition skills.
2. Acquire effective technical writing skills.
3. Prepare for placement and competitive exams
4. Facilitate effective English language skills for academic purposes.

Unit I: COMMUNICATIVE ENGLISH **9 Hours**
Introduction to Communicative English-Reading: Skimming and Scanning-Comprehensive questions- (Multiple choice questions/short questions/open-ended questions)-Speaking: Self-Introduction-Writing: Formal and informal letters (Requisition, Complaint/Invitation /Accepting/Declining/Personal) Grammar: Parts of speech, Present Tense-Vocabulary: Synonyms/Antonyms, word formation, Prefixes /suffixes.

Unit II: WORDS AND SENTENCES **9 Hours**
Reading: Reading biographies on famous scientists and personalities/ newspaper articles. Speaking: Travelog with pictorial video /PPT, Writing: Single line and extended definitions, Data interpretation (Pie chart, Bar chart, Table, Flow chart), Movie/book review. Grammar: Modal verbs, Voices, Past Tense Vocabulary: Compound words, One-word substitutions.

Unit III: TECHNICAL COMMUNICATION **9 Hours**
Reading: Review on technology/gadgets, reading user manual, Writing: Writing Instructions; Recommendations Speaking: Pride activity (About hometown) Grammar: Cause and Effect, Prepositions, Future Tense Vocabulary: Phrasal Verbs, Collocations.

Unit IV: BUSINESS COMMUNICATIONS **9 Hours**
Reading: Reading and understanding general and technical articles Writing: Report writing (Industrial visit report, Feasibility report), Checklist Speaking: Cultural and heritage of hometown, Dialogue writing and Telephonic conversation Grammar: WH questions, If conditionals Vocabulary: Abbreviation and Acronyms, Misspelt words.

Unit V: PROFESSIONAL ENGLISH **9 Hours**

Reading: Brochures, Scientific Blogs. Writing: Jumbled Sentences, Note-making Speaking: Team task (role play) Grammar: Types of sentences, Possessive case Vocabulary: Homonyms/ Homophones.

Course Outcomes (COs)

Upon completion of the course, students would be able to:

CO1: Make use of communicative English principles, reading strategies, and basic grammar rules to communicate effectively. (K3)

CO2: Apply grammar rules, sentence structures, vocabulary and interpret data to convey meaning accurately in spoken and written communication. (K3)

CO3: Utilize technical communication skills to read, write, and speak about technical topics, using appropriate vocabulary and grammatical structures. (K3)

CO4: Use business communication skills to read, write, and speak effectively in professional contexts, using appropriate formats, vocabulary, and tone. (K3)

CO5: Examine information from brochures and scientific blogs and participate in team tasks and role plays, communicating effectively. (K3)

Resources

1. Text Books

1. Corporate author; Department of English, Anna University. (2020). *English for Engineers & Technologists*. Orient Blackswan Private Ltd.
2. Ramalingam, N. (2013). *Grammar for all* (2nd ed.). Himalaya Publishing House.

2. Reference Books

1. Whitby, N. (2006). *Business Benchmark Pre-intermediate to intermediate Personal Study Book* (BEC and BULATS Edition). Cambridge University Press.
2. Laws, A. (2011). *Writing Skills*. Oxford Summertown.
3. Sinha, D. K. (2012). *Specimen of English Prose*. Orient BlackSwan.
4. Raman, M., & Sharma, S. (2009). *Technical Communication: Principles and Practice*. Oxford University Press.
5. Murphy, R. (2004). *English Grammar in Use* (4th ed.). Cambridge University Press.

3. E-Resources

1. American Association for the Advancement of Science. Science Blogs – Scientific Writing and Communication Perspectives.
   `https://www.science.org/blogs`
2. Liveworksheets. Interactive English Grammar and Communication Worksheets.
   `https://www.liveworksheets.com/worksheets/en`

3. Union Public Service Commission. Competitive Examination Communication and General English Guidelines.
`https://www.upsconline.nic.in/`

4. NPTEL. Technical English for Engineers – Lecture Notes and Modules.
`https://nptel.ac.in/courses/109106116`

5. Purdue University Online Writing Lab (OWL). Engineering Writing and Professional Communication Guidelines.
`https://owl.purdue.edu/owl/subject_specific_writing/creative_writing/index.html`

Industrial Relevance

In the global semiconductor and VLSI industry, technical competence must be matched by rigorous communication proficiencies. Engineers design complex hardware architectures that require clear articulation through architectural specifications, feasibility studies, and user manuals. This course bridges academic theory and industrial deployment by equipping students with essential skills in data interpretation, formal report writing, and professional correspondence. By mastering precise technical vocabulary and structured communication protocols, graduates can effectively present design trade-offs, collaborate across multidisciplinary engineering teams, and ensure seamless documentation standards during ASIC and FPGA development cycles worldwide.

CO-PO-PSO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	1	1	-	1	-	-	-	-	3	-	2	1	1	-
CO2	2	1	-	3	-	-	-	-	2	-	1	2	1	-
CO3	2	1	-	1	-	-	-	-	3	-	-	2	1	-
CO4	2	1	-	1	-	-	-	-	3	-	1	2	1	-
CO5	2	1	-	1	-	3	-	1	3	-	1	2	1	-
Weighted Average	1.80	1.00	-	1.40	-	3.00	-	1.00	2.80	-	1.25	1.80	1	-

Course Code: U23PYT01
Course Title: ENGINEERING PHYSICS
Course Type: Basic Sciences
L T P C: 3 0 0 3
Total Hours: 45
Pre-Requisite: -
SDG: 4,7,9

Course Overview

Engineering Physics establishes a comprehensive foundational framework encompassing classical mechanics, electromagnetic wave theory, quantum mechanics, and modern photonics essential for advanced electronic engineering analysis. The course systematically explores wave-particle duality, magnetic and superconducting material properties, and optical communication mechanisms to build a robust bridge between theoretical physical sciences and applied semiconductor technology. Mastery of these foundational physical principles empowers undergraduate students to analyze, conceptualize, and optimize nanoscale device behaviors, embedded electronic systems, and high-speed interconnects within the VLSI design ecosystem.

Course Objectives

To make the students:

1. Understand the fundamentals of mechanics.
2. Acquire the knowledge of electromagnetic waves.
3. Gain the knowledge of the magnetic and superconducting properties of materials.
4. Explore the principles of quantum mechanics and their applications.
5. Learn the principles of lasers and optical communication.

Unit I: MECHANICS **9 Hours**
Basic definitions – Multi–particle dynamics: Center of mass (CM) – CM of continuous bodies – motion of the CM – kinetic energy of the system of particles. Types of motion– Rotation of rigid bodies: Rotational kinematics – rotational kinetic energy – moment of inertia– torque – rotational dynamics of rigid bodies – conservation of angular momentum – rotational energy state of a rigid diatomic molecule – torsional pendulum.

Unit II: ELECTROMAGNETIC WAVES **9 Hours**
Basic definitions: Gauss law for electric field, Faraday's law and Ampere's circuit law – Maxwell's equations – Derivation of Maxwell's Equations – wave equation: Plane electromagnetic waves in vacuum – properties of electromagnetic waves in vacuum: speed, amplitude, phase, orientation and waves in matter – Energy and momentum in EM waves: Intensity, waves from localized sources, momentum and radiation pressure.

Unit III: MAGNETIC MATERIALS AND SUPERCONDUCTIVITY **9 Hours**
Introduction – Types of magnetic materials: Dia, Para and Ferromagnetism–domain theory of Ferromagnetism –hysteresis – Ferrites and application of Ferrites.
Superconductivity: Properties of Superconductor – Type I & Type II Superconductor. Application of Superconductor: Josephson junction – SQUID – Magnetic levitated Train.

Unit IV: QUANTUM PHYSICS **9 Hours**

Black body radiation(quantitative) – Compton effect: theory and experimental verification– matter waves – properties of matter waves –concept of wave function and its physical significance – Schrodinger's wave equation – time independent and time dependent equations –particle in a one–dimensional rigid box. Electron microscope– Scanning electron microscope.

Unit V: LASER AND FIBER OPTICS **9 Hours**

Lasers principles – Properties of Laser – Einstein's A and B coefficients derivation – Population inversion – resonant cavity– Types of Laser: He–Ne Laser – Semiconductor lasers – homo junction and hetero junction. Fiber optics: principle, numerical aperture and acceptance angle – types of optical fibers (material, refractive index, and mode). Fiber optic communication.

Course Outcomes (COs)

Upon completion of the course, students would be able to:

1. Apply the fundamental concepts of mechanics to analyze the motion of particles and rigid bodies, including rotational dynamics and energy states. (K3)
2. Apply maxwell's equations and fundamental laws to analyze electromagnetic wave propagation in vacuum and matter, including energy and momentum aspects. (K3)
3. Interpret the knowledge of magnetic and superconducting properties of materials and utilize the principles of superconductivity in squids and magnetic levitation. (K3)
4. Use quantum mechanics concepts and demonstrate their relevance in the functioning of electron microscopes. (K3)
5. Implement laser principles and optical fiber concepts to operate laser and optical fiber communication systems. (K3)

Resources

1. Text Books

1. Kleppner D and Kolenkow R, "An Introduction to Mechanics", 2017, McGraw Hill Education (Indian Edition), New Delhi.
2. Purcell E M and Morin D J, "Electricity and Magnetism", 2013, Cambridge University Press. United Kingdom.
3. Bhattacharya D.K and Poonam Tandon, "Engineering Physics", 2015, Oxford University Press, New Delhi.

2. Reference Books

1. Wolfson R, "Essential University Physics". Volume 1 & 2, 2020, Pearson Education (Indian Edition), New Delhi.
2. Halliday D, Resnick R and Walker J, "Physics". Volume 1 & 2, 2021, Wiley (Indian Edition), New Delhi.
3. Arthur Beiser, Shobhit Mahajan, Rai Choudhury S, "Concepts of Modern Physics", 2017, McGrawHill (Indian Edition), New Delhi.

3. E-Resources

1. NPTEL Course: Engineering Mechanics – Note: Rigid Body Dynamics and Motion Analysis
   `https://nptel.ac.in/courses/112107539`
2. NPTEL Course: Electromagnetic Theory – Note: Maxwell's Equations and EM Wave Propagation
   `https://nptel.ac.in/courses/115101005`
3. NPTEL Course: Solid State Physics – Note: Magnetic Materials and Superconductivity Fundamentals
   `https://nptel.ac.in/courses/115105131`
4. NPTEL Course: Quantum Mechanics I – Note: Wave Mechanics and Schrodinger Equation Applications
   `https://nptel.ac.in/courses/115102023`
5. NPTEL Course: Fiber Optics – Note: Laser Principles and Optical Fiber Communication Systems
   `https://nptel.ac.in/courses/113106064`

Industrial Relevance

Engineering Physics provides the essential material and quantum mechanical foundations required for state-of-the-art semiconductor manufacturing and VLSI device scaling. Understanding quantum wave functions and carrier dynamics is critical for designing nanometer-scale transistors, mitigating quantum tunneling leakage, and developing advanced gate-all-around architectures. Furthermore, electromagnetic wave theory and optical principles directly govern high-speed interconnect modeling, photolithography processes, and silicon photonics integration. By mastering these core physical phenomena, electronics engineering graduates are equipped to solve complex hardware optimization challenges and drive innovation across the global microelectronics and electronic design automation industries.

CO-PO-PSO Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	1	1	2	-	-	-	-	-	-	1	-	1
CO2	3	3	2	1	2	-	-	-	-	-	-	2	1	2
CO3	3	3	2	2	1	-	-	-	-	-	-	1	1	2
CO4	3	3	1	2	1	-	-	-	-	-	-	2	3	3
CO5	3	3	2	1	2	-	-	-	-	-	-	3	2	2
Weighted Average	3.00	3.00	1.60	1.40	1.60	-	-	-	-	-	-	1.80	1.75	2.0

Course Code: U23CST01
Course Title: Problem Solving and Programming in C
Course Type: Engineering Sciences
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: -
SDG: 4

Course Overview

This course provides a comprehensive foundation in structured programming principles and computational problem-solving methodologies using the ANSI C programming language. Key themes encompass algorithmic decomposition, control flow structures, modular program design through functions, memory manipulation via pointers, and persistent data management using files. Mastery of these core concepts is essential for VLSI design engineers to develop efficient firmware, hardware modeling tools, and electronic design automation scripts in semiconductor industries.

Course Objectives

To make the students:

1. Understand the fundamental concepts of problem solving and structured programming using the C language.
2. Develop C programs using decision-making, looping, arrays, strings, functions, and pointers.
3. Apply user-defined data types, file handling and dynamic memory management for solving computational problems.
4. Develop logical thinking and programming skills to design efficient solutions for real-world applications.

Unit I: PROBLEM SOLVING FUNDAMENTALS **9 Hours**
Fundamentals of Computing – Identification of Computational Problems -Problem solving- Flow Chart, Algorithm, Pseudo code – Introduction to C – Structure of a C program- Keyword-Identifiers - Data Types – Variables - Constants – Input/output statements Operators – Type Conversion and Type casting.

Unit II: CONDITIONAL STATEMENTS AND LOOPING CONSTRUCTS **9 Hours**
Conditional Branching Statements: if, if-else, else-if ladder, nested-if, switch constructs - Looping constructs: for, while, do-while constructs – Nested loops - Usage of break continue, return and go to statements.

Unit III: ARRAYS AND STRINGS **9 Hours**
1D Array –Declaration, Initialization, 2D Array - Declaration, Initialization – Operations on Arrays- Multi-dimensional Arrays, Strings: Declaration and Initialization - String operations: length, compare, concatenate, copy.

Unit IV: FUNCTIONS AND POINTERS **9 Hours**
Functions: Built-in Functions, User defined functions – Function Prototypes–Command Line

Arguments -Arrays and Functions – Strings and Functions- Scope of Variables – Storage classes – Recursion- Pointers: Declaration – Pointer operators – Pointer expressions -Passing Pointers to a Function – Pointers and one-dimensional arrays – Pointers and Strings - Dynamic Memory Allocation.

Unit V: STRUCTURES, UNIONS AND FILE HANDLING **9 Hours**

Structure: Creating a Structure-Member initialization - Accessing Structure Members - Nested structures – Pointer and Structures – Array of structures - Self Referential Structures – typedef –Unions – Bit fields – Enumerated data types - Files- Opening and Closing a Data File, Reading and writing a data file- Preprocessor Directives.

Course Outcomes

Upon completion of the course, students would be able to:

CO1: Apply problem-solving techniques and basic C programming constructs. (K3)

CO2: Implement conditional and looping statements for program control. (K3)

CO3: Utilize arrays and strings for data organization and processing. (K3)

CO4: Apply functions, pointers, and dynamic memory allocation to solve computational problems. (K3)

CO5: Develop applications using structures, unions, and file handling. (K3)

Resources

1. Text Books

1. Thareja, R. (2018). *Programming in C* (1st ed.). Oxford University Press.
2. Balagurusamy, E. (2019). *Programming in ANSI C* (8th ed.). McGraw-Hill Education.
3. Kernighan, B. W., & Ritchie, D. M. (1988). *The C Programming Language* (2nd ed.). Prentice Hall.

2. Reference Books

1. Gottfried, B. S. (2018). *Programming with C* (4th ed.). McGraw-Hill Education.
2. Kanetkar, Y. (2018). *Let Us C* (16th ed.). BPB Publications.
3. Deitel, P., & Deitel, H. (2016). *C How to Program* (8th ed.). Pearson Education.
4. Schildt, H. (2000). *C: The Complete Reference* (4th ed.). McGraw-Hill Education.

3. E-Resources

1. NPTEL. Problem Solving through Programming in C. Note: Covers basic algorithms, loop structures, and modular programming techniques.
   `https://onlinecourses.nptel.ac.in/e-learning/preview/noc22_cs40`
2. Udemy. C Programming For Beginners. Note: Comprehensive overview of syntax, pointers, and memory management fundamentals.
   `https://www.udemy.com/topic/c-programming/`

3. Coursera. C Programming Courses. Note: Vendor-neutral structured programming concepts and practical data organization methodologies.
   `https://www.coursera.org/courses?query=c%20programming`

4. NPTEL. Problem Solving and Programming in C. Note: Emphasizes data structures, pointer arithmetic, and file system interactions.
   `https://nptel.ac.in/courses/106105171`

5. NPTEL. Advanced C Programming. Note: Focuses on dynamic memory allocation, complex structures, and preprocessor usage.
   `https://onlinecourses.nptel.ac.in/e-learning/preview/noc26_cs155`

Industrial Relevance

In the semiconductor and VLSI design industries, proficiency in C programming is indispensable for electronic design automation (EDA) tool development, system-on-chip (SoC) verification, and embedded firmware engineering. Hardware engineers utilize C to write high-performance algorithmic models, behavioral simulations, and hardware-software co-design interfaces. Understanding memory management, pointers, and bit-level manipulations enables engineers to interact directly with hardware registers and optimize resource-constrained electronic architectures. This course bridges foundational computer science theory with practical hardware deployment, preparing students to build robust diagnostic drivers and test-bench environments essential for modern chip fabrication and testing workflows.

CO-PO-PSO Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	1	2	-	-	-	-	-	-	3	1	2
CO2	3	3	2	2	2	-	-	-	-	-	-	3	1	2
CO3	3	3	3	2	2	-	-	-	-	-	-	2	2	2
CO4	3	3	3	2	3	-	-	-	-	1	-	3	2	3
CO5	3	3	3	2	3	1	-	-	1	2	1	3	2	3
Weighted Average	3.00	2.80	2.60	1.80	2.40	1.00	-	-	1.00	1.50	1.00	2.80	1.60	2.40

Course Code: U23TAT01
Course Title: HERITAGE OF TAMILS
Course Type: Humanities and Social Sciences
L T P C: 1 0 0 1
Total Hours: 30
Pre-Requisites: -
SDG: 4
(Common to ALL branches)

Course Overview

This course provides an in-depth exploration of the rich linguistic, cultural, and historical evolution of the Tamil civilization, tracing its classical roots from the Sangam era to modern literature. Key themes encompass traditional arts, architectural heritage, indigenous systems of medicine, martial traditions, and the profound socio-cultural contributions of Tamils to the Indian freedom movement and global maritime trade. By instilling a strong foundation in heritage, traditional knowledge systems, and classical management principles from texts like Thirukkural, the curriculum fosters professional ethics, cultural awareness, and multidisciplinary problem-solving abilities vital for modern electronics and VLSI engineers.

Course Objectives

To make the students :

1. Understand the evolution of the tamil language, literature and their contribution to Indian civilization.
2. Gain knowledge of the cultural heritage, arts, architecture and traditions of the tamils.
3. Appreciate tamil folk arts, traditional games and their socio-cultural significance.
4. Understand the ecological, historical and economic aspects of ancient tamil society through sangam literature.
5. Recognize the contributions of tamils to the Indian freedom movement, medicine, education and culture.

Unit I: LANGUAGE AND LITERATURE **6 Hours**

Language Families in India-Dravidian Languages-Tamil as a Classical Language-Classical Literature in Tamil-Secular Nature of Sangam Literature- Distributive Justice in Sangam Literature-Management Principles in Thirukual-Tamil Epics and Impact of Buddhism & Jainism in Tamil Land-Bakthi Literature Azhwars and Nayanmars- Forms of minor Poetry-Development of Modern Literature in Tamil- Contribution of Bharathiyar and Bharathidasan.

Unit II: HERITAGE – ROCK ART PAINTINGS TO MODERN ART - SCULPTURE **6 Hours**

Hero stone to modern sculpture- Bronze icons-Tribes and their handicrafts-Art of temple car making- Massive Terracotta sculptures, Village deities,Thiruvalluvar Statue at Kanyakumari,Making of musical instruments-Mridhangam,Prai,Veenai, Yazh and Nadhaswaram-Role of Temples in Social and Economic life of Tamils.

Unit III: FOLK AND MARTIAL ARTS **6 Hours**

Therukoothu, Karagattam, Villu Pattu, Kaniyan Koothu, Oyillattam, Leather puppetry, Silambattam, Valari, Tiger dance – Sports and Games of Tamils.

Unit IV: THINAI CONCEPT OF TAMILS **6 Hours**

Flora and Fauna of Tamils & Aham and Puram Concept form Tholkappiyam and Sangam Literature – Aram Concept of Tamils-Education and Literacy during Sangam Age-Ancient Cities and Ports of Sangam Age-Export and Import during Sangam Age-Overseas Conquest of Cholas.

Unit V: CONTRIBUTION OF TAMILS TO INDIAN NATIONAL MOVEMENT AND INDIAN CULTURE **6 Hours**

Contribution of Tamils to Indian Freedom Struggle-The Cultural Influence of Tamils over the other parts of India- Self-Respect Movement – Role of Sidddha Medicine in Indigenous Systems of Medicine-Inscriptions & Manuscripts-Print History of Tamils Books.

Course Outcomes (COs)

Upon completion of the course, students would be able to :

CO1: Explain the evolution of the tamil language, classical literature and their significance in preserving tamil heritage. (K2)

CO2: Describe the traditional arts, architecture, sculpture, music and cultural practices of the tamils. (K2)

CO3: Illustrate the significance of tamil folk arts, traditional games and cultural practices in promoting social values and cultural identity. (K2)

CO4: Describe the ecological, historical, social and economic features of ancient tamil civilization through sangam literature. (K2)

CO5: Explain the contributions of tamils to the Indian freedom movement, education, medicine and Indian culture. (K2)

Resources

1. Text Books

1. Pillay, K. K. (2015). தமிழக வரலாறு - மக்களும் பண்பாடும் [*Tamizhaga Varalaru – Makkalum Panbadum*]. தமிழ்நாடு பாடநூல் மற்றும் கல்வி இயல் பணிகள் கழக வெளியீடு (Tamil Nadu Text Book and Educational Services Corporation).

2. Sundaram, L. (2018). கணினி தமிழ் [*Kanini Tamil*]. விகடன் பிரசுரம் (Vikatan Prasuram).

3. Department of Archaeology. (2019). கீழடி - வைகை நதி கரையில் சங்க கால நகர நாகரிகம் [*Keeladi – Sangam City Civilization on the Banks of River Vaigai*]. தொல்லியல் துறை வெளியீடு (Department of Archaeology, Government of Tamil Nadu).

4. Department of Archaeology. (2021). பொருநை - ஆற்றங்கரை நாகரீகம் [*Porunai – Atrangarai Nagarigam*]. தொல்லியல் துறை வெளியீடு (Department of Archaeology, Government of Tamil Nadu).

5. Pillay, K. K. (2020). *Social Life of Tamils*. A joint publication of TNTB & ESC and RMRL.

6. Singaravelu, S. (2001). *Social Life of the Tamils – The Classical Period*. International Institute of Tamil Studies.

2. Reference Books

1. Subatamanian, S. V., & Thirunavukkarasu, K. D. (1981). *Historical Heritage of the Tamils*. International Institute of Tamil Studies.

2. Valarmathi, M. (2012). *The Contributions of the Tamils to Indian Culture*. International Institute of Tamil Studies.

3. Department of Archaeology. (2020). *Keeladi – Sangam City Civilization on the banks of river Vaigai*. Jointly Published by Department of Archaeology & Tamil Nadu Text Book and Educational Services Corporation.

4. Pillay, K. K. (1975). *Studies in the History of India with Special Reference to Tamil Nadu*. The Author.

5. Department of Archaeology. (2021). *Porunai Civilization*. Jointly Published by Department of Archaeology & Tamil Nadu Text Book and Educational Services Corporation.

6. Balakrishnan, R. (2019). *Journey of Civilization: Indus to Vaigai*. Roja Muthiah Research Library (RMRL).

3. E-Resources

1. Tamil Virtual Academy. (2023). *Digital Library and History of Tamil Culture*. Note: Comprehensive digital repository of Sangam literature, ancient inscriptions, and classical heritage.
`https://www.tamilvu.org/`

2. Department of Archaeology, Government of Tamil Nadu. (2023). *Excavation Reports and Historical Heritage*. Note: Official archaeological findings tracing the urban civilization and antiquity of Tamil land.
`https://www.tnarch.gov.in/`

3. Tamil Digital Library. (2023). *Ancient Manuscripts and Rare Print Archives*. Note: Digitized manuscripts, palm-leaf archives, and print history of classical Tamil books.
`https://www.tamildigitallibrary.in/`

4. NPTEL. (2022). *History of Indian Science and Technology*. Note: Focuses on indigenous metallurgy, traditional architecture, and ancient water management systems.
`https://nptel.ac.in/courses/109104102`

5. Roja Muthiah Research Library (RMRL). (2023). *Indus to Vaigai: Archaeological and Linguistic Heritage Studies*. Note: Comparative research repository on Dravidian language families and early South Indian socio-economic history.
`https://rmrl.in/`

Industrial Relevance

Understanding the heritage of Tamils instills critical human values, ethical foundations, and classical management principles from texts like Thirukkural, which are essential for engineering leadership in the global semiconductor industry. Exploring ancient metallurgy, precision temple architecture, and sustainable water management fosters spatial reasoning and systems-thinking directly applicable to complex VLSI layout design and hardware architecture. Furthermore, analyzing traditional knowledge systems and the evolution of technical communication enhances multi-disciplinary teamwork, adaptability, and socio-environmental awareness required for developing sustainable, next-generation electronic technologies in diverse global engineering environments.

CO-PO-PSO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	-	-	-	-	-	-	-	1	-	1	-	-	-	1
CO2	-	-	-	-	-	-	-	1	-	1	-	-	-	1
CO3	-	-	-	-	-	-	-	1	-	1	-	-	-	1
CO4	-	-	-	-	-	-	-	2	1	1	-	-	-	1
CO5	-	-	-	-	-	-	-	2	1	1	-	-	-	1
Weighted Average	-	-	-	-	-	-	-	1.40	1.00	1.00	-	-	-	1.00

Course Code: U23PYP01
Course Title: Physics Laboratory
Course Type: Basic Sciences Laboratory
L T P C: 0 0 2 1
Total Periods: 30

Course Overview

This laboratory course provides hands-on experimental training in fundamental physical principles, establishing the measurement and instrumentation techniques essential for semiconductor device characterization. Learners develop practical skills in optics, mechanical elasticity, thermal conductivity, and electrical transport measurements through systematic data collection, graphical modeling, and error analysis. These foundational verification competencies directly support hardware analysis, material characterization, and optoelectronic troubleshooting in modern VLSI design, semiconductor manufacturing, and embedded communication industries.

Course Objectives

1. To learn the proper use of various kinds of physics laboratory equipment.
2. To learn how data can be collected, presented and interpreted in a clear and concise manner.
3. To learn problem solving skills related to physics principles and interpretation of experimental data.

Laboratory Experiments

Experiment 1: Determination of Wavelength of Laser.

Experiment 2: Determination of Particle Size and Acceptance angle of the fiber using laser.

Experiment 3: Determination of young's modulus by Uniform bending.

Experiment 4: Determination of thickness of a thin wire by Air wedge method.

Experiment 5: Determination of thermal conductivity of bad conductor.

Experiment 6: Determination of Rigidity modulus by Torsion pendulum.

Experiment 7: Determination of wavelength of mercury spectrum Spectrometer grating.

Experiment 8: Determination of bandgap of a semiconductor.

Experiment 9: Determination of specific resistance of a given coil of wire Carey Foster Bridge.

Course Outcomes (COs)

CO1: Use the different components and equipment in physics practical. (K3)

CO2: Solve problems individually and summarize the experimental results effectively. (K3)

CO3: Use graphical models to analyze laboratory data and develop skills to impart practical knowledge in real time solution. (K3)

Resources

1. Text Books

1. Kleppner, D., & Kolenkow, R. (2017). *An Introduction to Mechanics.* McGraw Hill Education (Indian Edition), New Delhi.
2. Purcell, E. M., & Morin, D. J. (2013). *Electricity and Magnetism.* Cambridge University Press, United Kingdom.
3. Bhattacharya, D. K., & Tandon, P. (2015). *Engineering Physics.* Oxford University Press, New Delhi.

2. Reference Books

1. Wolfson, R. (2009). *Essential University Physics* (Vols. 1-2). Pearson Education (Indian Edition), New Delhi.
2. Halliday, D., Resnick, R., & Walker, J. (2015). *Principles of Physics.* Wiley (Indian Edition), New Delhi.
3. Beiser, A., Mahajan, S., & RaiChoudhury, S. (2017). *Concepts of Modern Physics.* McGraw Hill (Indian Edition), New Delhi.

3. E-Resources

1. Virtual Physics Laboratory on Physical and Mechanical Measurements. Note: Optical diffraction and mechanical modulus simulation procedures.
   `http://vlab.amrita.edu/?sub=1&brch=281`
2. Virtual Laboratory on Semiconductor Physics. Note: Bandgap determination and resistivity measurement protocols.
   `http://vlab.amrita.edu/?sub=1&brch=195`
3. Virtual Laboratory on Advanced Optics. Note: Spectrometer grating and laser numerical aperture analysis.
   `http://www.vlab.co.in/broad-area-physical-sciences`
4. NPTEL Course on Experimental Physics. Note: Instrumentation calibration, error analysis, and data plotting methodologies.
   `https://archive.nptel.ac.in/courses/115/105/115105110/`

5. MIT OpenCourseWare Physics Laboratory. Note: Fundamental physical measurements, validation, and verification techniques.
   `https://ocw.mit.edu/courses/8-013-physics-i-classical-mechanics-fall-2016/`

Industrial Relevance

This foundational physics laboratory course bridges fundamental scientific theory with rigorous industrial deployment practices across semiconductor, communication, embedded systems, and VLSI sectors. By engaging in precision optical and electrical measurements, learners master core instrumentation skills—such as operating spectrometers, traveling microscopes, and precision bridge networks—that directly underpin semiconductor wafer metrology and thin-film characterization in fabrication foundries. Hardware implementation skills are honed through the physical assembly of test circuits for bandgap determination and specific resistance evaluation, mirroring circuit debugging and parameter extraction workflows in Electronic Design Automation (EDA) device modeling. Furthermore, experiments involving laser fiber optics and numerical aperture measurements simulate essential communication system testing protocols required for validating optical interconnects and high-speed signal transmission. The emphasis on systematic data logging, graphical error analysis, and parameter verification equips future VLSI engineers with the critical validation and verification techniques necessary to troubleshoot complex integrated circuits and optimize physical device performance on silicon.

CO-PO-PSO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	2	-	1	-	1	1	-	-	-	1	-	-
CO2	3	3	2	-	1	-	2	1	-	-	-	2	2	-
CO3	3	3	1	-	1	-	2	1	-	-	-	2	2	2
Weighted Average	3.00	3.00	1.67	0.00	1.00	0.00	1.67	1.00	0.00	0.00	0.00	1.67	2.00	2.00

Course Code: U23CSP01
Course Title: Problem Solving and Programming in C Laboratory
Course Type: Engineering Science Laboratory
L T P C: 0 0 2 1
Total Hours: 30
Prerequisite(s):
SDG:4

Course Overview

This laboratory course aims to develop comprehensive competence in fundamental and modular C programming through hands-on computational problem-solving. Students will develop practical skills in writing structured code, manipulating arrays and strings, implementing modular functions with pointers, and performing file handling operations. Mastering these foundational programming constructs provides the essential algorithmic framework required for firmware development, hardware-software co-design, and Electronic Design Automation (EDA) tool scripting in the semiconductor and VLSI industries.

Course Objectives

1. To write and execute basic C programs applying input/output statements, operators, expressions, and decision-making constructs to solve foundational engineering problems.
2. To implement modular programming techniques using functions, arrays, strings, and pointers for efficient data manipulation and memory access.
3. To construct comprehensive applications utilizing structures, unions, and file handling mechanisms to store, read, and process persistent data.

Laboratory Experiments

Experiment 1: I/O statements, operators, expressions.

Experiment 2: Decision-making constructs: if-else, go to, switch-case, break-continue.

Experiment 3: Loops: for, while, do-while.

Experiment 4: Arrays: 1D and 2D, multi-dimensional arrays.

Experiment 5: Strings: Operations.

Experiment 6: Functions: call, return, passing arrays to function, Passing string to functions, Recursion.

Experiment 7: Pointers: Pointers to Functions, Arrays and Strings, Passing parameters to functions.

Experiment 8: Structures: Nested Structures, Pointers to Structures, Arrays of Structures and Unions.

Experiment 9: Files: reading and writing, File pointers, File operations, Preprocessor directives.

Experiment 10: Mini project.

Course Outcomes

Upon completion of the course, students would be able to:

CO1:
Apply fundamental C programming constructs to develop programs. (K3)

CO2:
Develop modular C programs using functions, pointers, structures, and file handling. (K3)

CO3:
Build applications by integrating C programming concepts to solve computational problems. (K3)

Resources

Text Books

1. Gottfried, B. S. (2018). *Programming with C* (4th ed.). McGraw-Hill Education.
2. Thareja, R. (2016). *Programming in C* (2nd ed.). Oxford University Press.

Reference Books

1. Kernighan, B. W., & Ritchie, D. M. (1988). *The C programming language* (2nd ed.). Prentice Hall.
2. Prata, S. (2013). *C primer plus* (6th ed.). Addison-Wesley Professional.

E-Resources

1. IIIT Hyderabad. (2026). *Problem solving lab in C*. Virtual Labs. `https://cse02-iiith.vlabs.ac.in/List%20of%20experiments.html`
2. LabEx. (2026). *Free C programming labs*. `https://labex.io/free-labs/c`
3. NPTEL. (2023). *Problem solving through programming in C*. Indian Institute of Technology Kharagpur. `https://nptel.ac.in/courses/106105171`
4. GNU Project. (2023). *The GNU C reference manual*. Free Software Foundation. `https://www.gnu.org/software/gnu-c-manual/`
5. MIT OpenCourseWare. (2011). *Practical programming in C*. Massachusetts Institute of Technology. `https://ocw.mit.edu/courses/6-087-practical-programming-in-c-january-iap-2011/`

Industrial Relevance

This laboratory course develops critical measurement, instrumentation, hardware implementation, and circuit debugging skills by establishing a robust mathematical and algorithmic foundation through C programming. In the semiconductor, embedded systems, and VLSI industries, low-level programming is indispensable for firmware development, communication system testing, register-level hardware manipulation, and developing verification testbenches. By mastering modular code architecture, pointer-based memory access, and file I/O operations, students

acquire the precise analytical and validation techniques required to build custom Electronic Design Automation (EDA) scripts, interface with test and measurement instrumentation, and debug complex hardware-software boundaries in modern System-on-Chip (SoC) architectures.

CO–PO–PSO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	2	1	2	-	-	-	-	-	-	3	2	-
CO2	3	3	3	2	3	-	-	-	-	-	-	3	3	2
CO3	3	3	3	2	3	1	-	-	-	-	1	3	3	3
Weighted Average	3.00	2.67	2.67	1.67	2.67	1.00	-	-	-	-	1.00	3.00	2.67	2.50

Course Code: U23MEP02
Course Title: ENGINEERING DRAWING
Course Type: Engineering Science Laboratory
L T P C: 0 0 4 2
Total Hours: 60
Prerequisite(s): Nil
SDG: 4,9

Course Overview

This laboratory course provides an essential foundation in technical drafting, spatial visualization, and geometric modeling required for communicating complex engineering concepts and designs. Students develop practical proficiency in generating standardized 2D multi-view orthographic projections, sectional views, surface developments, and 3D isometric models using both manual sketching techniques and industry-standard computer-aided drafting (CAD) software. The competencies acquired directly support downstream industry workflows in electronic packaging, VLSI hardware layout, embedded system chassis design, and electro-mechanical component verification.

Course Objectives

To make the students:

- Develop graphic skills for communication of concepts, ideas and design of engineering products.
- Expose them to existing national BIS standards related to technical drawings.
- Master the generation of precise 2D orthographic and 3D isometric representations using manual drafting and industry-standard modeling software.

Laboratory Exercises

1: Construction of Ellipse, Parabola and Hyperbola using Eccentricity method. To draw tangent and normal to the above curves at any point.

2: Construction of Cycloid and Involute curves with tangent and normal at any point on the curve.

3: Projection of simple solids (Prism, Pyramid, Cylinder and Cone) when the axis is inclined to one of the principal planes by rotating object method.

4: Sectioning of solids (Prism, Pyramid, Cylinder and Cone) in simple vertical position when the cutting plane is inclined to the one of the principal planes and perpendicular to the other.

5: Development of lateral surfaces of simple solids – Prisms, pyramids, cylinders and cones.

6: Free Hand sketching: Sketching of multiple views from pictorial views of objects.

7: Isometric projections of simple solids - Prisms, pyramids, cylinders, cones- combination of two solid objects in simple vertical positions.

8: Study of capabilities of software for Drafting and Modeling – Coordinate systems (absolute, relative, polar, etc.) – Creation of simple figures like polygon and general multi-line figures.

9: Drawing of curves like parabola, spiral, involute using B-spline or cubic spline.

10: Drawing of front view and top view of simple solids like prism, pyramid, cylinder and cone including dimensioning.

11: Drawing front view, top view and side view of objects from the given pictorial views.

12: Drawing isometric projection of simple objects.

Course Outcomes

Upon completion of the course, students would be able to:

CO1: Prepare orthographic projections of simple solids inclined to the principal planes, using standard drawing conventions. **(K3)**

CO2: Sketch lateral surface developments of sectioned solids and generate 2D multi-view drawings from given 3D models. **(K3)**

CO3: Construct isometric views from given 3D models with correct proportions and dimensions. **(K3)**

Resources

Text Books

1. Venugopal, K., & Prabhu Raja, V. (2019). *Engineering Graphics.* New Age International (P) Limited, New Delhi.

2. Natarajan, K. V. (2018). *A text book of Engineering Graphics.* Dhanalakshmi Publishers, Chennai.

3. Bhatt, N. D., & Panchal, V. M. (2019). *Engineering Drawing* (53rd ed.). Charotar Publishing House, Ahmedabad.

Reference Books

1. Agrawal, B., & Agrawal, C. M. (2013). *Engineering Drawing.* Tata McGraw Hill Education Private Limited, New Delhi.

2. Narayana, K. L., & Kannaiah, P. (2008). *Text book on Engineering Drawing* (2nd ed.). Scitech Publications (India) Pvt. Ltd., Chennai.

3. Luzzader, W. J., & Duff, J. M. (2001). *Fundamentals of Engineering Drawing* (11th ed.). Prentice-Hall of India Pvt. Ltd., New Delhi.

E-Resources

1. NPTEL Course on Engineering Graphics and Design: `https://nptel.ac.in/courses/112103019`
2. MIT OpenCourseWare - Design and Manufacturing I: `https://ocw.mit.edu/courses/2-007-design-and-manufacturing-i-spring-2009/`
3. Bureau of Indian Standards (BIS) - SP 46: Engineering Drawing Practice for Schools and Colleges: `https://www.bis.gov.in/`
4. IEEE Xplore Digital Library - CAD and Modeling Standards: `https://ieeexplore.ieee.org/`
5. Open-Source 2D CAD Documentation and Tutorials (LibreCAD / QCAD): `https://librecad.org/`

Industrial Relevance

In contemporary engineering workflows, precise graphical communication is foundational to successful product design, component verification, and system integration. For professionals in Electronics Engineering, Embedded Systems, and VLSI Design, mastery of technical drafting and spatial geometry is indispensable when designing physical enclosures, custom printed circuit board (PCB) form factors, heat sinks, and electromechanical interfaces. Proficiency in constructing sectioned views and lateral surface developments ensures accurate manufacturing of sheet metal shielding and packaging hardware. Furthermore, hands-on experience with coordinate systems, spline generation, and parametric CAD modeling tools directly bridges the gap between conceptual schematic layout and physical hardware fabrication, enabling engineers to collaborate effectively across multidisciplinary industrial teams.

CO–PO–PSO Articulation Matrix

Cos	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	2	3	-	-	3	3	1	1	3	2	-
CO2	2	2	2	2	3	-	-	3	3	1	1	3	2	-
CO3	2	2	2	2	3	-	-	3	3	1	1	3	2	-
Weighted Average	**2.00**	**2.00**	**2.00**	**2.00**	**3.00**	**-**	**-**	**3.00**	**3.00**	**1.00**	**1.00**	**3.00**	**2.00**	**-**

Course Code: U23MAT02
Course Title: Transforms and Boundary Value Problems
Course Type: Basic Sciences
Pre-Requisites: Linear Algebra and Calculus
L T P C: 3 1 0 4
Total Hours: 60
Common to CIVIL, ECE,EEE,MECH,MCT and EE(VDT)
SDG : 4,7,9

Course Objectives

1. Understand the basic concepts of partial differential equations for solving standard types.
2. Learn fourier series in engineering problems.
3. Acquaint with fourier transform techniques used in wide variety of situations.
4. Interpret with fourier series techniques in solving heat flow problems.
5. Develop effective mathematical tools for the solutions of partial differential equations to model several physical processes and to learn z transform techniques for discrete time systems.

Unit I: PARTIAL DIFFERENTIAL EQUATIONS **9+3 Hours**
Solution of standard types of first order equations - Lagrange's equation - linear partial Differential equation of second and higher order with constant coefficients.

Unit II: FOURIER SERIES **9+3 Hours**
Dirichlet's conditions - General Fourier series - Half Range Sine and Cosine series - Parseval's Identity - Harmonic Analysis.

Unit III: FOURIER TRANSFORM **9+3 Hours**
The infinite Fourier transform pair - sine and cosine transform - properties - Parseval's identity and convolution theorem (statement only).

Unit IV: BOUNDARY VALUE PROBLEMS **9+3 Hours**
Classification of Second order linear partial differential equations - solutions of one-dimensional wave equation - One-dimensional heat equation, steady state solution of two-dimensional heat equation, Fourier series solution in cartesian coordinates.

Unit V: Z - TRANSFORMS **9+3 Hours**
Definition and properties - Elementary Problems - Inverse Z transforms (partial fraction method) - convolution theorem (statement only) - Application of Z Transforms in solving difference equations.

Course Outcomes (COs)

Upon completion of the course, students would be able to:

CO1: Solve the standard partial differential equations. (K3)

CO2: Solve differential equations using Fourier series analysis in engineering applications. (K3)

CO3: Apply the mathematical principles of transforms and partial differential equations to formulate and solve the physical problems of engineering. (K3)

CO4: Apply the physical significance of Fourier series techniques in solving one and two-dimensional heat flow problems and one-dimensional wave equations. (K3)

CO5: Apply the mathematical tools for the solutions of partial differential equations using the z transform techniques for discrete time systems. (K3)

Resources

1. Text Books

1. Grewal, B. S., & Grewal, J. S. (2022). *Higher Engineering Mathematics* (45th ed.). Khanna Publishers, New Delhi.

2. Kreyszig, E. (2018). *Advanced Engineering Mathematics* (10th ed.). John Wiley and Sons (Asia) Ltd, Delhi.

2. Reference Books

1. Bali, N. P., & Goyal, M. (2015). *A Textbook of Engineering Mathematics* (10th ed.). Laxmi Publications Pvt Ltd.

2. Ramana, B. V. (2019). *Higher Engineering Mathematics* (7th ed.). McGraw Hill Education Pvt. Ltd, New Delhi.

3. James, G. (2018). *Advanced Modern Engineering Mathematics* (5th ed.). Pearson Education, New Delhi.

3. E-Resources

1. NPTEL Course: Advanced Engineering Mathematics (Note: Partial Differential Equations and Fourier Series), IIT Roorkee.
   `https://nptel.ac.in/courses/111102129`

2. NPTEL Course: Mathematics - III (Note: Fourier Transforms and Boundary Value Problems), IIT Guwahati.
   `https://nptel.ac.in/courses/111103021`

3. NPTEL Course: Transform Techniques for Engineers (Note: Z-Transforms and Difference Equations), IIT Madras.
   `https://nptel.ac.in/courses/111108144`

4. MIT OpenCourseWare: Differential Equations and Linear Algebra (Note: Fourier Series and PDE Applications), Massachusetts Institute of Technology.
   `https://ocw.mit.edu/courses/18-03-differential-equations-spring-2010/`

5. NPTEL Course: Partial Differential Equations (Note: One-Dimensional Wave and Heat Flow Equations), IIT Bombay.
   `https://nptel.ac.in/courses/111101053`

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	-	3	2	-	-	-	-	-	1	3	1	1
CO2	3	3	-	3	2	-	-	-	-	-	1	3	2	1
CO3	3	3	-	3	2	-	-	-	-	-	1	3	2	2
CO4	3	3	-	3	2	-	-	-	-	-	2	3	2	2
CO5	3	3	-	2	3	-	-	-	-	-	2	3	2	2
Weighted Average	3.00	3.00	-	2.80	2.2	-	-	-	-	-	1.40	3.00	1.80	1.60

Course Code: U23CYT01
Course Title: Engineering Chemistry
Course Type: Basic Sciences
L T P C: 3 0 0 3
Total Hours: 45
Pre-Requisites: -
SDG: 6,7,9
Common to CSE, CSE (CS), CSE(AI&ML), ECE, EEE, EE(VDT), AI&DS and IT

Course Overview

This course equips students with essential chemical principles governing water technology, electrochemistry, energy storage, polymers, and nanomaterials critical for modern engineering applications. By exploring the chemical foundations of materials and electrochemical processes, the curriculum establishes a direct connection between molecular behavior and macroscopic device performance in electronic and semiconductor systems. Ultimately, students gain the analytical capability to select, treat, and synthesize advanced materials required for next-generation hardware and VLSI technologies.

Course Objectives

To make the students:

1. Understand water quality parameters and different water treatment techniques.
2. Conversant with the basic knowledge of electrochemistry and corrosion.
3. Familiarise with the operating principles, working processes and applications of energy conversion and storage devices.
4. Understand the preparation, properties and uses of various polymers.
5. Familiarize with the basic knowledge on the principles and preparatory methods of nanomaterials.

Unit I: WATER TECHNOLOGY **9 Hours**

Hardness of water-types -expression-units-estimation of hardness of water by EDTA-numerical problems-boiler feed water-disadvantages of hard water in boilers-boiler troubles (scale & sludge, boiler corrosion)-water treatment-zeolite process, Ion exchange process-desalination-reverse osmosis-instrumental methods for water analysis-AAS, flame emission spectroscopy and photocolorimetry.

Unit II: ELECTROCHEMISTRY AND CORROSION **9 Hours**

Electrochemical cell-reversible and irreversible cell-electrode potential-electrochemical series-Nernst equation (derivation and problems)-reference electrode-calomel electrode, ion selective electrode-glass electrode-emf -measurement of emf of a cell- Electrochemical sensors. Corrosion-types-chemical, electrochemical corrosion (galvanic, differential aeration)-corrosion control-sacrificial anodic method and impressed current cathodic protection method. Protective coatings -electroplating of gold and electroless plating of nickel-paints-constituents and functions.

Unit III: ENERGY SOURCES AND STORAGE DEVICES **9 Hours**

Energy sources-types-nuclear energy-nuclear fission-controlled nuclear fission-nuclear fusion-nuclear reactor power generator-breeder reactor-solar energy-solar energy conversion-wind energy Batteries - primary (alkaline battery) - Secondary (lead storage battery, NICAD battery and lithium ionbattery) -Electric vehicles – working principles -Fuel cells (H2-O2 , direct methanol and solid oxide)-super capacitors.

Unit IV: POLYMERS **9 Hours**

Polymers: functionality, degree of polymerisation, molecular weight Mn and Mw-classification-types of polymerisation-glass transition temperature-factors affecting Tg- industrially important polymers-preparation, properties and uses of PE, PET, PU, Nylon, epoxy resin-Printed circuit board-Flexible electronics – conducting polymers (intrinsic and extrinsic). Organic electronic materials (introduction only)-applications.

Unit V: NANO MATERIALS **9 Hours**

Nano Chemistry: Basics-distinction between molecules, nanoparticles and bulk materials-preparation of nanoparticles by sol-gel-preparation of nanowires by electro spinning-preparation of carbon nanotube by chemical vapour deposition-quantum dots-synthesis by colloidal process- Applications of nanomaterials in medicine, agriculture, energy, electronics and catalysis.

Course Outcomes (COs)

CO1: Infer the quality of water from quality parameter data and propose suitable treatment methodologies to treat water. (K3)
CO2: Employ fundamental principles of corrosion science to identify and implement effective corrosion protection techniques across diverse engineering applications. (K3)
CO3: Demonstrate the working principles and applications of batteries in portable devices, backup power supplies, and electric vehicles. (K3)
CO4: Make use of polymer chemistry fundamentals to identify and meet future material fabrication requirements. (K3)
CO5: Apply the basic concepts of nanochemistry to identify appropriate nanomaterials and synthesis techniques for engineering and technological applications. (K3)

Resources

1. Text Books

1. Jain, P. C., & Jain, M. (2018). *Engineering chemistry* (17th ed.). Dhanpat Rai Publishing Company (P) Ltd, New Delhi.

2. Palanna, O. G. (2017). *Engineering chemistry* (2nd ed.). McGraw Hill Education (India) Pvt. Ltd.

3. Dara, S. S., & Umare, S. S. (2020). *A text book of engineering chemistry* (20th ed.). S. Chand Publishing, New Delhi.

2. Reference Books

1. Murty, B. S., Shankar, P., Raj, B., Rath, B. B., & Murday, J. (2018). *Text book of nanoscience and nanotechnology*. Universities Press (India) Pvt. Ltd.

2. Sivasankar, B. (2008). *Engineering chemistry-fundamentals and applications*. Tata McGraw-Hill Publishing Company, Ltd., New Delhi.

3. Agarwal, S. (2019). *Engineering chemistry* (2nd ed.). Cambridge University Press, New Delhi.

3. E-Resources

1. NPTEL Course – Note: Water Quality and Treatment Methodology
   `https://nptel.ac.in/courses/105107207`
2. NPTEL Course – Note: Electrochemistry and Corrosion Control
   `https://nptel.ac.in/courses/104106137`
3. NPTEL Course – Note: Energy Storage and Battery Technology
   `https://nptel.ac.in/courses/113104082`
4. NPTEL Course – Note: Polymer Chemistry and Flexible Electronics
   `https://nptel.ac.in/courses/113105102`
5. NPTEL Course – Note: Nanochemistry and Synthesis of Nanomaterials
   `https://nptel.ac.in/courses/104105124`

Industrial Relevance

Modern VLSI manufacturing and hardware packaging rely fundamentally on principles of chemical engineering and material science. This course directly addresses industry demands by mastering ultrapure water generation critical for wafer cleaning, electrochemistry essential for electroplating interconnects, and corrosion prevention in semiconductor packaging. Furthermore, knowledge of specialized polymers enables the design of advanced printed circuit boards and flexible electronics, while nanochemistry principles govern the synthesis of nanomaterials and quantum dots used in cutting-edge semiconductor devices. By bridging core chemical theory with chip fabrication and device packaging, students gain foundational skills necessary for semiconductor hardware deployment.

CO-PO-PSO Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	1	1	-	-	-	-	-	-	-	1	1
CO2	3	1	1	1	1	1	-	-	-	-	-	-	2	1
CO3	3	1	1	-	-	1	-	-	-	-	-	1	-	1
CO4	3	1	1	-	-	1	-	-	-	-	-	1	2	2
CO5	3	-	2	-	1	1	-	-	-	-	-	1	3	2
Weighted Average	3.00	1.25	1.20	1.00	1.00	1.00	-	-	-	-	-	1.00	2.00	1.40

Course Code: U23CST02
Course Title: Python Programming
Course Type: Engineering Science
L T P C: 3 0 0 3
Total Hours: 45
Prerequisite's : -
SDG: 4
Common to All branches

Course Overview

This course establishes a robust foundation in general-purpose programming using high-level data structures, algorithmic logic, and object-oriented paradigms. Key themes encompass modular program architecture, sequence manipulation, exception handling, and persistent data operations essential for complex hardware-software co-design. In the realm of VLSI design and technology, these fundamental programming competencies are indispensable for automating verification workflows, parsing testbench data, and scripting electronic design automation processes without relying on proprietary vendor tools.

Course Objectives

To make the students:

1. Understand the fundamentals of Python programming.
2. Develop Python programs using data structures, functions, modules, packages, and object-oriented programming concepts.
3. Build Python applications using file and exception handling techniques.

Unit I: BASICS OF PYTHON PROGRAMMING **9 Hours**
Introduction to Python - Python Interpreter – Data types - variables - expressions -statements- Operators and Expressions – Strings – Decision control statements

Unit II: PYTHON DATA STRUCTURES **9 Hours**
Sequence - Lists - Functional Programming – Tuples – Sets- Dictionaries

Unit III: FUNCTIONS, MODULES AND PACKAGES **9 Hours**
Functions – Definition – Call - Variable scope and Life time – Return- Lambda Functions- Recursive functions- Modules – Packages

Unit IV: OBJECT ORIENTED PROGRAMMING **9 Hours**
Object-Oriented Concepts and Terminology - Classes and objects - Attributes and Methods - Inheritance – Method overriding – Data encapsulation – Data hiding

Unit V: FILES AND EXCEPTION HANDLING **9 Hours**
File Handling - Read - Write – Command Line Programming – Exception Handling

Course Outcomes

Upon completion of the course, students would be able to:

CO1. Develop Python programs using data types and control structures. (K3)

CO2. Utilize Python data structures to solve computational problems. (K3)

CO3. Develop structured Python programs using functions, modules, and packages. (K3)

CO4. Apply object-oriented programming concepts to develop Python applications. (K3)

CO5. Develop Python applications using file handling and exception handling. (K3)

Resources

1. Text Books

1. Downey, A. B. (2016). *Think Python: How to think like a computer scientist* (2nd ed.). O'Reilly Media (Shroff Publishers & Distributors Pvt. Ltd.).
2. Thareja, R. (2018). *Problem solving and programming with Python* (1st ed.). Oxford University Press.
3. Liang, Y. D. (2017). *Introduction to programming using Python* (1st ed.). Pearson Education.

2. Reference Books

1. Lambert, K. A. (2012). *Fundamentals of Python: First programs.* Cengage Learning.
2. Dierbach, C. (2013). *Introduction to computer science using Python: A computational problem-solving focus.* Wiley India Pvt. Ltd.
3. Sedgewick, R., Wayne, K., & Dondero, R. (2016). *Introduction to programming in Python: An inter-disciplinary approach.* Pearson India Education Services Pvt. Ltd.
4. Matthes, E. (2019). *Python crash course: A hands-on, project-based introduction to programming* (2nd ed.). No Starch Press.

3. E-Resources

1. NPTEL Course: Programming, Data Structures and Algorithms using Python. Note: Focuses on foundational data structures and functional programming algorithms.
   `https://nptel.ac.in/courses/106106145`
2. SWAYAM/CEC Course: Problem Solving and Programming in Python. Note: Covers core interpreter concepts, decision control statements, and procedural logic.
   `https://onlinecourses.swayam2.ac.in/cec22_cs20/preview`
3. NPTEL Course: Joy of Computing using Python. Note: Illustrates algorithmic problem solving, matrix operations, and basic object-oriented principles.
   `https://nptel.ac.in/courses/106106182`
4. Complete Beginner's Modular Programming Portal. Note: Comprehensive tutorials on variable scope, lambda functions, and user-defined packages.
   `https://www.udemy.com/course/python-for-complete-beginners-1/`
5. Official Python Documentation and Tutorial Portal. Note: Standard reference for file handling, command-line arguments, and exception handling protocols.
   `https://docs.python.org/3/tutorial/index.html`

Industrial Relevance

In modern semiconductor and VLSI engineering, automation is critical for reducing design-to-silicon turnaround times. While core hardware description occurs in specialized design languages, high-level programming serves as the backbone for electronic design automation infrastructure. Engineers utilize modular scripting, object-oriented data modeling, and robust file handling to parse massive simulation log files, automate verification suites, and generate layout-versus-schematic regression reports. Mastering vendor-neutral programmatic logic allows hardware engineers to build customized toolchains and optimize complex testing workflows across the global semiconductor ecosystem.

CO-PO-PSO Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	1	2	-	-	-	-	-	-	2	1	2
CO2	3	3	2	2	2	-	-	-	-	-	-	3	2	2
CO3	3	3	3	2	3	-	-	-	-	1	-	3	2	3
CO4	3	3	3	2	3	-	-	-	-	1	-	3	2	3
CO5	3	3	3	2	3	1	-	-	1	2	1	3	3	3
Weighted Average	3.00	2.80	2.60	1.80	2.60	1.00	-	-	1.00	1.33	1.00	2.80	2.00	2.60

Course Code: U23ECT01
Course Title: Electric Circuits and Electron Devices
Course Type: Engineering Sciences
L T P C: 3 0 0 3
Total Periods 45
Prerequisites: Engineering Physics

Course Overview

This course provides a comprehensive foundation in the analysis of DC and AC electrical circuits and the operational physics of semiconductor devices. It explores essential network theorems, semiconductor energy band structures, and the functional characteristics of various electronic components. Students will gain the analytical skills required to model and evaluate circuit behavior, forming a critical basis for advanced studies in VLSI design and microelectronics.

Course Objectives

1. To apply fundamental circuit laws and network theorems for the analysis of DC and AC electrical networks.
2. To understand the physics of semiconductors and the operational characteristics of junction devices.
3. To evaluate the performance and applications of special-purpose semiconductor diodes and power control devices.

Unit I: BASIC CIRCUITS CONCEPTS **9 Periods**
Ohm's Law - Kirchoff's laws DC and AC Circuits - Resistors in series and parallel circuits - Mesh current and node voltage method of analysis for D.C and A.C. circuits.
Unit II: NETWORK REDUCTION AND NETWORKS THEOREMS FOR DC AND AC CIRCUITS **9 Periods**
Network reduction: voltage and current division - source transformation - Thevenin's and Norton Theorem - Superposition Theorem - star delta conversion - Maximum power transfer theorem - Reciprocity Theorem.
Unit III: THEORY OF SEMICONDUCTOR **9 Periods**
Energy band diagram of semiconductor - Charge carriers in semiconductors - Extrinsic semiconductor - Charge neutrality - Position of Fermi energy level - Electron-Hole generation and recombination - Conductivity - Temperature dependence drift and diffusion current - Poisson equation and Continuity equation.
Unit IV: PN JUNCTION DIODE AND TRANSISTORS **9 Periods**
PN Junction diode - BJT structure and operation - JFET - Comparison of BJT and FET - Characteristics of JFET - Enhancement MOSFET - Depletion MOSFET.
Unit V: SPECIAL SEMICONDUCTOR DIODES **9 Periods**
Zener diodes - Varactor diode - Tunnel diodes - DIAC - TRIAC - SCR - Photo diodes - Photo transistors - LED.

Course Outcomes (COs)

CO1: Apply Kirchoff's laws and their application with simple series and parallel resistive circuits. (K3)

CO2: Solve electrical network problems using mesh and nodal analysis and by applying network theorems. (K3)
CO3: Extend the knowledge of semiconductor. (K4)
CO4: Construct different types of diodes and transistors, operation and its characteristics. (K3)
CO5: Make use of special diodes to understand the operation and their characteristics. (K3)

Resources

1. Text Books

1. Salivahanan. S and Suresh Kumar N., "Electronic Devices and Circuits", 2008, McGraw Hill Education.
2. Joseph A. Ed'minister, Mahmood, Nahri, "Electric Circuits", 2001, Shaum series, TataM-cGraw Hill.
3. ÖzgürErgül, "Introduction to Electrical Circuit Analysis", 2017, Wiley.
4. David A. Bell, "Electronic Devices and Circuits", 5th Edition, 2008, Oxford University Press.

2. Reference Books

1. Floyd, "Electron devices", 2001, Pearson Asia 5th Edition.
2. Singh B.P, Rekha Singh, "Electronics Devices and Circuits", 2003, Pearson Second Edition.
3. Arumugam M. and Premkumar N, "Electric Circuit Theory", 1991, Kanna Publishers.
4. Sudhakar A. and Shyam Mohan S.P, "Circuits and Networks: Analysis and Synthesis", 2015 Tata McGraw-Hill Education (India) Pvt Ltd, New Delhi.

3. E-Resources

1. NPTEL Basic Circuit Analysis
   `https://nptel.ac.in/courses/108105159`
2. NPTEL Electronic Devices
   `https://nptel.ac.in/courses/108108122`
3. NPTEL Semiconductor Physics
   `https://onlinecourses.nptel.ac.in/noc21_ee80/preview`
4. OpenCourseWare Circuits and Electronics
   `https://ocw.mit.edu/courses/6-002-circuits-and-electronics-spring-2007/`
5. Semiconductor Device Fundamentals Documentation
   `https://ieeexplore.ieee.org/browse/standards`

Industrial Relevance

This course bridges the gap between theoretical electrical principles and the physical realities of modern semiconductor manufacturing. By mastering circuit reduction and device physics, students are prepared to understand the behavior of transistors and integrated circuits, which are the fundamental building blocks of all hardware systems. This knowledge is essential for professional roles in semiconductor fabrication, hardware verification, and integrated circuit design, aligning with current industrial requirements for sustainable and efficient device architecture.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	0	0	0	0	0	0	0	0	2	2	0	0
CO2	3	2	2	0	0	0	0	0	0	0	2	2	0	0
CO3	2	2	3	0	0	0	0	0	0	0	2	2	0	0
CO4	3	3	3	3	0	2	0	0	2	2	2	2	2	0
CO5	2	3	1	0	0	0	0	0	0	0	0	0	0	2
Weighted Average	2.60	2.60	2.25	3.00	0.00	2.00	0.00	0.00	2.00	2.00	2.00	2.00	2.00	2.00

Course Code: U23EGT02
Course Title: Professional English
Course Type: Humanities and Social Sciences
L T P C: 3 0 0 3
Total Hours: 45
Pre-Requisites: -
SDG: 4,8,9
Common to ALL branches

Course Overview

This course is designed to equip undergraduate engineering students with foundational and advanced linguistic competencies required for effective communication in global professional environments. Key themes encompass creative thinking, professional vocabulary enhancement, technical writing, business correspondence, and standardized proficiency preparation such as IELTS and TOEFL. Mastery of these communication skills is crucial for VLSI design engineers to articulate complex hardware architectures, draft rigorous technical specifications, and collaborate seamlessly across international multidisciplinary teams.

Course Objectives

1. Communicate clearly and confidently in professional environment.
2. Draft professional documents with clarity and accuracy.
3. Strengthen domain specific vocabulary and workplace interaction skills.
4. Equip with interview skills and international competitive exams.

Unit I: CREATIVE THINKING **9 Hours**
Articles – Conjunctions – Sentence Pattern - subject-verb agreement - Sentence completions-online worksheets on matching, Compare and contrast any topic in about 150 words eg. Vehicle vs E-Vehicle, Teacher vs Robot Teachers.

Unit II: PROFESSIONAL VOCABULARY **9 Hours**
Punctuation- Expansion of Compound nouns- Idioms and Phrases- Process description, product description, Letter Format- Job application and resume writing -Online worksheets for hints development.

Unit III: TECHNICAL SKILL **9 Hours**
Discourse Markers - Gerunds and infinitive – Relative Pronouns – Definitions of Technical Terms – Digital Transcoding – Group discussion (Do's and Don'ts)- Minutes of Meeting, online worksheet on transcoding.

Unit IV: BUSINESS COMMUNICATIONS **9 Hours**
Clauses – Phrases – Numerical Adjectives – Complaint Letter-Filling up forms (Opening bank a/c and ticket booking) – Virtual Communication: E-Mail Writing – Essay Writing: Types of essays Opinion Essay, Discussion Essay, Direct Questions Essay, Advantage/Disadvantage Essay, Problem/Solution Essay.

Unit V: PROFESSIONAL ENGLISH **9 Hours**
TOEFL / IELTS- (LSRW) Synonyms; Vocabulary; reading comprehension of IELTS/ TOEFL; Writing exercises of IELTS/ TOFEL, Verbal Ability, Use and purpose expression, travel itinerary.

Course Outcomes (COs)

CO1. Use grammatical structures proficiently to produce professional written expressions and critically compose accurate paragraphs. (K3)

CO2. Demonstrate product descriptions with precision and draft resumes using guided terminology. (K3)

CO3. Use technical communication competencies to articulate complex ideas with precision and clarity and participate effectively in group discussions. (K3)

CO4. Construct in formal content for letters, emails and structured essays. (K3)

CO5. Apply language competencies effectively for competitive examinations and professional pursuits. (K4)

Resources

1. Text Books

1. Department of English, Anna University. (2020). *English for Engineers & Technologists*. Orient Blackswan Private Ltd.
2. Ramalingam, N. (2013). *Grammar for all* (2nd ed.). Himalaya Publishing House.

2. Reference Books

1. Whitby, N. (2006). *Business Benchmark Pre-intermediate to intermediate Personal Study Book* (BEC and BULATS Edition). Cambridge University Press.
2. Laws, A. (2011). *Writing Skills*. Oxford, Summertown Publishing.
3. Sinha, D. K. (2012). *Specimen of English Prose*. Orient Black Swan.
4. Raman, M., & Sharma, S. (2009). *Technical Communication: Principles and Practice*. Oxford University Press.
5. Murphy, R. (2004). *English Grammar in Use* (4th ed.). Cambridge University Press.

3. E-Resources

1. NPTEL Course: Technical English for Engineers – IIT Bombay. Note: Covers grammar, technical vocabulary, and workplace communication protocols.
   `https://nptel.ac.in/courses/109106094`
2. NPTEL Course: Developing Soft Skills and Personality – IIT Kanpur. Note: Focuses on group discussions, interpersonal skills, and interview preparation.
   `https://nptel.ac.in/courses/109104107`
3. British Council: LearnEnglish Professionals. Note: Provides interactive worksheets and exercises for business correspondence and email writing.
   `https://learnenglish.britishcouncil.org/business-english`
4. Purdue Online Writing Lab (OWL): Technical Writing and Engineering Documentation. Note: Offers guidelines on process descriptions, resume drafting, and formal letter formatting.
   `https://owl.purdue.edu/owl/subject_specific_writing/professional_technical_writing/index.html`

5. Science Magazine Blogs and Editorial Resources. Note: Advanced reading comprehension, analytical essay models, and discourse analysis for technical sciences.
   `https://www.science.org/blogs`

Industrial Relevance

In the global semiconductor and VLSI engineering sector, technical excellence must be matched by impeccable communication skills. Engineers frequently collaborate across multinational design centers to develop intricate ASIC specifications, articulate complex verification plans, and draft patent disclosures. This course bridges academic linguistic principles with industry demands by mastering precise technical vocabulary, digital transcoding, and formal design documentation. Furthermore, preparation for international proficiency standards and structured group discussions empowers graduates to navigate technical design reviews, contribute to global standard-setting bodies, and excel in competitive leadership roles within the fabless and semiconductor manufacturing industries.

CO-PO-PSO Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	1	1	-	-	-	-	-	-	3	-	-	-	-	1
CO2	1	1	-	-	-	-	-	-	3	-	1	-	-	2
CO3	1	1	-	1	-	-	-	1	3	-	1	-	-	2
CO4	1	1	-	-	-	-	-	-	3	-	1	-	-	1
CO5	1	-	-	-	-	-	-	-	3	-	1	-	-	2
Weighted Average	1.00	1.00	-	1.00	-	-	-	1.00	3.00	-	1.00	-	-	1.60

Course Code: U23TAT02
Course Title: TAMILS AND TECHNOLOGY
Course Type: Humanities and Social Science
L T P C: 1 0 0 1
Total Hours: 30
Pre-Requisites: -
SDG: 4
Common to ALL branches

Course Overview

This course explores the rich historical heritage, scientific knowledge, and indigenous technological advancements achieved by the ancient Tamil civilization across diverse engineering disciplines. Key themes encompass traditional manufacturing in metallurgy and ceramics, structural architecture and irrigation systems, and the modern evolution of scientific Tamil alongside digital computing resources. By investigating these time-tested sustainable practices and computational linguistic tools, engineering students gain critical insights into historical innovation that inspire modern hardware design and localized technology development.

Course Objectives

1. Understand the technological advancements of the tamils in weaving, pottery, architecture and construction.
2. Gain knowledge of the production technologies, metallurgy, shipbuilding and manufacturing practices of ancient tamils.
3. Understand the traditional agricultural and irrigation technologies adopted by the tamils.
4. Recognize the scientific knowledge and technological innovations reflected in tamil civilization.
5. Understand the development of scientific tamil, computational tamil and tamil digital resources.

Course Contents

Unit I: WEAVING AND CERAMIC TECHNOLOGY **6 Hours**
Weaving Industry during Sangam Age - Ceramic Technology - Black and Red Ware Potteries (BRW) - Graffiti on Potteries - Raw materials used in ancient looms - Natural dye extraction and application techniques - Kiln design and temperature control in pottery - Structural durability of ancient ceramics - Social and economic impact of textile trade.

Unit II: DESIGN AND CONSTRUCTION TECHNOLOGY **6 Hours**
Designing and Structural construction House & Designs in household materials during Sangam Age - Building materials and Hero stones of Sangam Age - Details of Stage Constructions in Silappathikaram - Sculptures and Temples of Mamallapuram - Great Temples of Cholas and other worship places - Temples of Nayaka Period - Type study (Madurai Meenakshi Temple) - Thirumalai Nayakar Mahal - Chetti Nadu Houses, Indo-Saracenic architecture at Madras during British Period.

Unit III: MANUFACTURING TECHNOLOGY **6 Hours**
Art of Ship Building - Metallurgical studies - Iron industry - Iron smelting, steel - Copper and

gold - Coins as source of history - Minting of Coins - Beads making-industries Stone beads - Glass beads - Terracotta beads - Shell beads/bone beads - Archeological evidences - Gem Stone types described in Silappathikaram.

Unit IV: AGRICULTURE AND IRRIGATION TECHNOLOGY **6 Hours**
Dam, Tank, ponds, Sluice, Significance of Kumizhi Thoompu of Chola period - Animal Husbandry - Wells designed for cattle use - Agriculture and Agro Processing - Knowledge of Sea - Fisheries - Pearl - Conche diving - Ancient Knowledge of Ocean - Knowledge Specific Society.

Unit V: SCIENTIFIC TAMIL & TAMIL COMPUTING **6 Hours**
Development of Scientific Tamil - Tamil computing - Digitalization of Tamil books - Development of Tamil Software - Tamil Virtual Academy - Tamil Digital Library - Online Tamil Dictionaries - Sorkuvai Project - Natural language processing for Tamil script and typography.

Course Outcomes (COs)

Upon completion of the course, students would be able to:

CO1: Explain the traditional technologies adopted by the tamils in weaving, pottery, architecture, and construction. (K2)

CO2: Describe the production technologies, metallurgy, shipbuilding and manufacturing practices of ancient tamils. (K2)

CO3: Explain the agricultural, irrigation and marine technologies practiced by the tamils. (K2)

CO4: Describe the scientific knowledge and technological developments reflected in tamil civilization. (K2)

CO5: Explain the evolution of scientific tamil, computational tamil and tamil digital technologies. (K2)

Resources

1. Text Books

1. கே.கே. பிள்ளை, ""தமிழக வரலாறு - மக்களும் பண்பாடும்", தமிழ்நாடு பாடநூல் மற்றும் கல்வி இயல் பணிகள் கழக வெளியீடு (Pillay, K. K., *History of Tamil Nadu - People and Culture*, Tamil Nadu Textbook and Educational Services Corporation).

2. முனைவர் இல. சுந்தரம், ""கணினி தமிழ்", விகடன் பிரசுரம் (Sundaram, L., *Computational Tamil*, Vikatan Prasuram).

3. ""கீழடி - வைகை நதி கரையில் சங்க கால நகர நாகரிகம்", தொல்லியல் துறை வெளியீடு (*Keeladi - Sangam City Civilization on the Banks of River Vaigai*, Department of Archaeology, Government of Tamil Nadu).

4. ""பொருநை - ஆற்றங்கரை நாகரீகம்", தொல்லியல் துறை வெளியீடு (*Porunai - River Bank Civilization*, Department of Archaeology, Government of Tamil Nadu).

2. Reference Books

1. Pillay, K. K. (2015). *Social Life of Tamils*. TNTB & ESC and RMRL.
2. Singaravelu, S. (2001). *Social Life of the Tamils - The Classical Period*. International Institute of Tamil Studies.
3. Subramanian, S. V., & Thirunavukkarasu, K. D. (1981). *Historical Heritage of the Tamils*. International Institute of Tamil Studies.
4. Valarmathi, M. (2012). *The Contributions of the Tamils to Indian Culture*. International Institute of Tamil Studies.
5. Department of Archaeology. (2019). *Keeladi - Sangam City Civilization on the banks of river Vaigai*. Department of Archaeology & Tamil Nadu Textbook and Educational Services Corporation, Tamil Nadu.
6. Pillay, K. K. (1975). *Studies in the History of India with Special Reference to Tamil Nadu*. The Author.
7. Department of Archaeology. (2021). *Porunai Civilization*. Department of Archaeology & Tamil Nadu Textbook and Educational Services Corporation, Tamil Nadu.
8. Balakrishnan, R. (2019). *Journey of Civilization Indus to Vaigai*. RMRL.

3. E-Resources

1. Tamil Virtual Academy - Digital Library and Online Learning Portal: `https://www.tamilvu.org/`
2. Department of Archaeology, Government of Tamil Nadu - Archaeological Reports: `https://www.tnarch.gov.in/`
3. Tamil Digital Library - Digital Archive of Ancient and Modern Tamil Literature: `https://www.tamildigitallibrary.in/`
4. NPTEL Course: Indian Culture and Heritage (Note: Focus on Dravidian Architecture): `https://nptel.ac.in/courses/109104102`
5. Project Madurai - Open Access Digital Archive of Tamil Literary Works: `https://www.projectmadurai.org/`

CO-PO-PSO Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	-	-	-	-	-	1	-	-	-	1	-	-	-	-
CO2	-	-	-	-	-	1	-	-	-	1	-	-	1	-
CO3	-	-	-	-	-	1	-	-	-	1	-	-	-	-
CO4	-	-	-	-	-	2	1	1	-	1	-	-	-	1
CO5	-	-	-	-	-	2	1	-	-	1	-	1	-	1
Weighted Average	-	-	-	-	-	1.40	1.00	1.00	-	1.00	-	1.00	1.00	1.00

Industrial Relevance

This course connects ancient material science and manufacturing heritage with modern semiconductor and hardware engineering practices. Studying historical advancements in metallurgy, precision bead fabrication, and structural thermodynamics provides VLSI engineers with foundational insights into material durability and sustainable design. Furthermore, the exploration of scientific Tamil and computing directly supports modern localization of Electronic Design Automation (EDA) interfaces, digital typography, and natural language processing in embedded hardware systems. This intersection of classical engineering heritage and computational linguistics fosters holistic, context-aware hardware engineers capable of developing indigenous technological solutions for global semiconductor markets.

Course Code: U23CYP01
Course Title: Chemistry Laboratory
Course Type: Engineering Science Laboratory
L T P C: 0 0 2 1
Total Hours: 30
Prerequisite(s):-
SDG: 6,9

Course Overview

This laboratory course imparts practical knowledge in evaluating critical water quality parameters and determining trace impurities through advanced volumetric and instrumental analysis. Students develop essential experimental skills utilizing electro-analytical techniques such as pH-metry, potentiometry, and conductometry, alongside viscometric evaluation of polymers. The practical competencies acquired are directly relevant to semiconductor, communication, and VLSI industries for maintaining ultra-pure water standards and analyzing chemical materials used in cleanroom fabrication environments.

Course Objectives

To make the students:

- Acquire practical skills in determination of water quality parameters through volumetric and instrumental analysis.
- Develop experimental skills to analyze water quality parameters, including acidity, hardness and dissolved oxygen (DO).
- Determine the molecular weight of a polymer using viscometry techniques.
- Familiarize with electro analytical techniques such as pH metry, potentiometry and conductometry in the determination of impurities in aqueous solutions.

Laboratory Experiments

Experiment 1: Estimation of Total, Temporary and Permanent Hardness of Water Sample by EDTA method

Experiment 2: Determination of DO content in Water by Winkler's method

Experiment 3: Determination of strength of acids in a mixture using conductivity meter

Experiment 4: Determination of strength of acid in a base using conductivity meter

Experiment 5: Determination of strength of an acid using pH meter

Experiment 6: Estimation of iron content of the given solution using potentiometer

Experiment 7: Determination of molecular weight and degree of polymerisation of a polymer (PVA) by viscometric method

Experiment 8: Estimation of Iron in a given sample by photo colorimetry

Course Outcomes

Upon completion of the course, students would be able to:

CO1: Analyse the quality of water samples with respect to their hardness and DO. (K3)

CO2: Quantitatively analyse the impurities in solution by electroanalytical techniques. (K3)

CO3: Determine the amount of metal ions by spectroscopic techniques and molecular weight of polymers by viscometric method. (K3)

Resources

Reference Books

1. Vogel, A. I., Mendham, J., Denney, R. C., Barnes, J. D., & Thomas, M. (2017). *Vogel's textbook of quantitative chemical analysis* (6th ed.). Pearson Education India.

E-Resources

1. Amrita Vishwa Vidyapeetham. (n.d.). *Virtual labs: Physical chemistry and analytical chemistry lab.*
   `https://vlab.amrita.edu/`
2. National Institute of Standards and Technology. (n.d.). *NIST chemistry webbook.*
   `https://webbook.nist.gov/`
3. Royal Society of Chemistry. (n.d.). *Analytical chemistry practical techniques and procedures.*
   `https://www.rsc.org/`
4. American Chemical Society. (n.d.). *Journal of chemical education: Laboratory experiments and methods.*
   `https://pubs.acs.org/journal/jceda8`
5. Massachusetts Institute of Technology. (n.d.). *MIT OpenCourseWare: Experimental chemistry techniques.*
   `https://ocw.mit.edu/`

Industrial Relevance

This laboratory course provides foundational exposure to rigorous analytical measurement, high-precision instrumentation skills, and systematic chemical validation techniques that are critical across modern engineering sectors. In the semiconductor, embedded systems, and VLSI industries, cleanroom fabrication facilities rely heavily on Ultra-Pure Water (UPW) systems; the experimental competencies gained in hardness analysis, dissolved oxygen determination, and electro-analytical impurity tracking directly mirror industrial quality control protocols used to prevent gate oxide degradation and wafer contamination. Furthermore, hands-on experience

with potentiometric, conductometric, and photo-colorimetric instrumentation establishes strong troubleshooting and circuit debugging fundamentals, as students learn to calibrate sensors, interpret electrical responses from physical phenomena, and verify system integrity against stringent industrial standards.

CO–PO–PSO Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	-	1	-	1	2	-	1	-	-	1	3	-	1
CO2	3	1	2	-	1	2	-	1	-	-	-	3	-	2
CO3	3	1	2	-	1	2	-	1	-	-	-	3	1	1
Weighted Average	3.00	1.00	1.67	-	1.00	2.00	-	1.00	-	-	1.00	3	1.00	1.67

Course Code: U23CSP02

Course Title: PYTHON PROGRAMMING LABORATORY

Course Type: Engineering Science Laboratory

L T P C: 0 0 2 1

Total Hours: 30

Prerequisite(s): Problem Solving and C Programming (or Equivalent Fundamental Computing Course)
SDG: 4

Course Overview

This laboratory course aims to develop proficiency in Python programming through the practical implementation of programming constructs, object-oriented programming, data structures, and file handling techniques. Students develop essential practical skills in algorithmic problem-solving, modular script development, data manipulation, and error debugging through hands-on coding and experimentation. Proficiency in Python scripting is directly relevant to the electronics, communication, and VLSI industries for automating Electronic Design Automation (EDA) workflows, hardware verification, and electronic test instrumentation.

Course Objectives

1. To apply foundational Python programming constructs, conditional statements, and iterative loops to solve computational engineering problems.
2. To implement modular programs utilizing functions, string manipulations, built-in data structures, standard libraries, file handling, and exception handling techniques.
3. To build real-world engineering applications by integrating Object-Oriented Programming (OOP) concepts and project-based problem-solving methodologies.

Laboratory Experiments

Experiment 1: Python programming using simple statements and expressions (CO1)

Experiment 2: Conditionals and Iterative loops

Experiment 3: Implementing programs using Functions.

Experiment 4: Implementing programs using Strings

Experiment 5: Implementing real-time/technical applications using Lists, Tuples, and Dictionaries.

Experiment 6: Implementing programs using written modules and Python Standard Libraries.

Experiment 7: Implementing real-time/technical applications using File handling.

Experiment 8: Implementing real-time/technical applications using Exception handling.

Experiment 9: Python programming using OOPs concepts

Experiment 10: Mini project.

Course Outcomes

Upon completion of the course, students would be able to:

CO1: Apply Python programming constructs to solve computational problems. (K3)

CO2: Develop Python programs using functions, object-oriented programming, standard libraries, file handling, and exception handling. (K3)

CO3: Build Python applications by integrating programming concepts to solve real-world problems. (K3)

Resources

Text Books

1. Downey, A. B. (2024). *Think Python: How to think like a computer scientist* (3rd ed.). O'Reilly Media.
2. Guttag, J. V. (2021). *Introduction to computation and programming using Python: With application to computational modeling and understanding data* (3rd ed.). MIT Press.

Reference Books

1. Lutz, M. (2013). *Learning Python: Powerful object-oriented programming* (5th ed.). O'Reilly Media.
2. Matthes, E. (2023). *Python crash course: A hands-on, project-based introduction to programming* (3rd ed.). No Starch Press.

E-Resources

1. `https://python-iitk.vlabs.ac.in/`
2. `https://docs.python.org/3/tutorial/index.html`
3. `https://nptel.ac.in/courses/106106182`
4. `https://www.scipy-lectures.org/`
5. `https://www.w3schools.com/python/`

Industrial Relevance

In the modern semiconductor, embedded systems, communication, and VLSI industries, Python has established itself as the primary scripting language for engineering automation, hardware validation, and instrumentation control. This laboratory course develops critical measurement and instrumentation skills by empowering students to write scripts that interact with automated test equipment, parse measurement datasets, and execute measurement logging. Through structured troubleshooting and debugging tasks, students acquire circuit debugging and verification

competencies necessary for evaluating communication system performance and validating complex VLSI architectures. Furthermore, mastery of data structures, file handling, and Object-Oriented Programming (OOP) directly supports Electronic Design Automation (EDA) script development, layout design rule check (DRC) automation, and automated testbench generation, thereby bridging software engineering methodologies with physical chip design and hardware implementation workflows.

CO–PO–PSO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	2	1	2	-	-	-	-	-	-	2	1	1
CO2	3	3	3	2	3	-	-	-	-	1	-	3	2	2
CO3	3	3	3	2	3	1	-	-	1	2	1	3	3	3
Weighted Average	**3.00**	**2.67**	**2.67**	**1.67**	**2.67**	**1.00**	**-**	**-**	**1.00**	**1.50**	**1.00**	**2.67**	**2.00**	**2.00**

Course Code: U23ECP04
Course Title: Electric Circuit and Electron Devices Laboratory
Course Type: Engineering Sciences Laboratory
L T P C: 0 0 2 1
Total Periods: 30
Prerequisite(s): Basic Knowledge of Physics

Course Overview

This laboratory course provides students with practical experience in analyzing electric circuits and characterizing fundamental electronic devices. Students develop essential skills in hardware implementation, circuit debugging, and measurement using standard laboratory instrumentation. These competencies are foundational for professional practice in the electronics, communication, and VLSI industries.

Course Objectives

1. To gain hands on experience in Thevenin& Norton theorem, KVL & KCL, and Superposition Theorems.
2. To learn the characteristics of PN Junction diode and Zener diode.
3. To learn the characteristics of basic electronic devices such as Diode, BJT, FET, SCR.

Laboratory Experiments

Experiment 1: Study of Electronic Components (CO1)
Experiment 2: Verification of KVL and KCL (CO2)
Experiment 3: Verification of Thevenin's and Norton's Theorem (CO2)
Experiment 4: Verification of Superposition Theorem (CO2)
Experiment 5: Characteristics of PN Junction diode (CO3)
Experiment 6: Characteristics of FET (CO3)
Experiment 7: Characteristics of Zener diode (CO3)
Experiment 8: Characteristics of Photo diodes and photo transistor (CO3)
Experiment 9: Characteristics of SCR (CO3)

Course Outcomes

CO1: Infer the characteristics of basic electronic devices (K2)
CO2: Verify Thevenin& Norton theorem KVL & KCL, and Super Position Theorems (K3)
CO3: Analyse Characteristics of PN Junction Diode, FET and special diodes (K4)

Resources

Text Books

1. Salivahanan S. and Suresh Kumar N., "Electronic Devices and Circuits", (2008) McGraw Hill Education.
2. Joseph A. Ed'minister, Mahmood, Nahri, "Electric Circuits", (2001) Shaum series, Tata McGraw Hill.

3. David A. Bell, "Electronic Devices and Circuits", 5th Edition, (2008) Oxford University Press.
4. Özgür Ergül, "Introduction to Electrical Circuit Analysis", (2017) Wiley.

Reference Books

1. Floyd, "Electron devices", 5th Edition, (2001) Pearson Asia.
2. Singh B.P. and Rekha Singh, "Electronics Devices and Circuits", 2nd Edition, 2003 Pearson.
3. Arumugam M. and Premkumar N, "Electric Circuit Theory", (1991) Kanna Publishers.
4. Sudhakar A. and Shyam Mohan S.P, "Circuits and Networks: Analysis and Synthesis", 2015, Tata McGraw-Hill Education (India) Pvt Ltd, New Delhi.

E-Resources

`https://www.nptelvideos.com/course.php?id=64`
`https://www.electronics-tutorials.ws/`
`https://www.allaboutcircuits.com/`
`https://www.circuitlab.com/blog/`
`https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/`

Industrial Relevance

This laboratory develops critical measurement and instrumentation skills through hands-on hardware implementation and rigorous circuit testing. By focusing on validation and verification techniques, students gain proficiency in circuit debugging and signal analysis. These practical abilities are directly applicable to semiconductor fabrication, communication system testing, embedded systems design, and complex VLSI circuit performance optimization.

CO–PO–PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	-	-	-	-	-	-	-	-	-	-	2	2	3
CO2	3	3	-	3	2	-	-	-	-	2	2	2	3	-
CO3	3	3	3	-	-	-	-	-	2	-	1	1	-	-
Weighted Average	2.67	3.00	3.00	3.00	2.00	-	-	-	2.00	2.00	1.50	1.67	2.50	3.00

Course Code: U23MAT06
Course Title: PROBABILITY AND RANDOM PROCESSES
Course Type: Basic Science
L T P C: 3 1 0 4
Total Hours: 60
Pre-Requisites: -
SDG: 4,9

Course Overview

This course provides a comprehensive foundational framework in probability theory, random variables, and stochastic processes essential for modeling complex engineering systems. Key themes encompass one-dimensional and two-dimensional random variables, standard probability distributions, Markov processes, correlation functions, and spectral densities. In the context of VLSI design and technology, these analytical concepts are indispensable for statistical static timing analysis, semiconductor noise modeling, and linear time-invariant system analysis in communication hardware.

Course Objectives

To make the students:

1. Understand the basic concepts in probability and random processes for applications such as random signals, linear systems in communication engineering.
2. Exemplify the basic concepts of probability, one-dimensional random variable and some standard distributions that are applicable to engineering problems which can describe real life Phenomenon.
3. Acquire more knowledge in two-dimensional random variables and correlation.
4. Interrupt the basic concepts of random processes used widely in signals and systems.
5. Equip the concept of correlation and spectral densities and the significance of linear systems with random inputs.

Course Contents

Unit I: PROBABILITY AND RANDOM VARIABLES **9+3 Hours**
Probability – Axioms of probability – Conditional probability –Baye's Theorem- Discrete and continuous random variables – Moments – Moment generating functions.

Unit II: ONE – DIMENSIONAL RANDOM VARIABLE **9+3 Hours**
Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions-Transformation of one dimensional random variables.

Unit III: TWO – DIMENSIONALRANDOM VARIABLES **9+3 Hours**
Joint distributions – Marginal and conditional distributions – Covariance – Correlation and linear regression.

Unit IV: RANDOM PROCESSES AND MARKOV PROCESSES **9+3 Hours**
Classification – Stationary process – Markov process - Markov chain - Poisson process.

Unit V: CORRELATION, SPECTRAL DENSITIES AND LINEAR SYSTEMS WITH RANDOM INPUTS **9+3 Hours**

Auto correlation functions – Cross correlation functions – Properties – Power spectral density – Cross spectral density – Properties. Linear time invariant system – System transfer function – Linear systems with random inputs – Auto correlation and cross correlation functions of input and output.

Course Outcomes

Upon completion of the course, students would be able to:

CO1. Use the fundamental knowledge of the concepts of probability. (K3)

CO2. Employ the knowledge of standard distributions. (K3)

CO3. Utilize the basic concepts of two-dimensional random variables to engineering Applications. (K3)

CO4. Implement the concept random processes and markov processes. (K3)

CO5. Demonstrate the concepts of correlation and spectral densities and utilize various distribution functions for handling linear time-invariant systems. (K3)

Resources

1. Text Books

1. Ibe, O. C. (2014). *Fundamentals of applied probability and random processes* (2nd ed., Indian Reprint). Elsevier.
2. Peebles, P. Z. (2002). *Probability, random variables and random signal principles* (4th ed.). Tata McGraw Hill.

2. Reference Books

1. Ramana, B. V. (2019). *Higher engineering mathematics* (7th ed.). McGraw Hill Education (India).
2. Cooper, G. R., & McGillem, C. D. (2012). *Probabilistic methods of signal and system analysis* (3rd Indian ed.). Oxford University Press.
3. Miller, S. L., & Childers, D. G. (2012). *Probability and random processes with applications to signal processing and communications* (2nd ed.). Academic Press.

3. E-Resources

1. NPTEL Course: Probability and Random Variables / Processes for Wireless Communications – Note: Fundamentals of random variables and signal processing.
   `https://nptel.ac.in/courses/117105085`
2. NPTEL Course: Probability and Random Processes – Note: Stationary processes, Markov chains, and linear systems.
   `https://nptel.ac.in/courses/108103185`

3. NPTEL Course: Probability and Statistics – Note: Standard distributions, joint distributions, and correlation.
   `https://www.nptel.ac.in/courses/111105041`

4. NPTEL Course: Principles of Communication Systems – Note: Power spectral density, noise analysis, and random inputs.
   `https://nptel.ac.in/courses/108104091`

5. MIT OpenCourseWare: Probabilistic Systems Analysis and Applied Probability – Note: Axioms of probability, transform methods, and Markov processes.
   `https://ocw.mit.edu/courses/6-041-probabilistic-systems-analysis-and-applied-probabili`

Industrial Relevance

As semiconductor devices scale into deep sub-micron regimes, deterministic models become insufficient due to severe process, voltage, and temperature variations. This course bridges fundamental stochastic theory with modern hardware engineering practices by enabling statistical static timing analysis and parametric yield estimation in chip manufacturing. Furthermore, concepts such as power spectral density, correlation functions, and Markov processes are vital for analyzing thermal noise, modeling channel interference in on-chip communication interconnects, and verifying linear time-invariant hardware blocks. Mastery of these probabilistic techniques allows VLSI engineers to design resilient, high-performance integrated circuits that meet rigorous industrial reliability and yield standards.

CO-PO-PSO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	-	1	2	-	-	-	-	-	1	2	-	1
CO2	3	3	-	1	2	-	-	-	-	-	-	2	-	1
CO3	3	3	-	1	2	-	-	-	-	-	-	2	-	1
CO4	3	3	-	2	2	-	-	-	-	-	-	3	1	2
CO5	3	3	1	2	2	-	-	-	-	-	-	3	1	2
Weighted Average	3.00	3.00	1.00	1.40	2.00	-	-	-	-	-	1.00	2.40	1.00	1.40

Course Code: U23CST03
Course Title: Data Structures
Course Type: Engineering Science
L T P C: 3 0 0 3
Total Periods: 45
Prerequisites: Problem solving and Programming in C

Course Overview

This course provides a comprehensive foundation in abstract data types and their implementation for efficient data management in engineering applications. It explores the design and application of linear and non-linear data structures, alongside critical analysis of sorting, searching, and hashing techniques. The curriculum enables students to select and implement appropriate algorithmic structures for complex hardware-software co-design problems.

Course Objectives

1. To understand the concept of Abstract Data Types (ADTs).
2. To understand the concepts and applications of Linear and Non-Linear Data Structures.
3. To identify the right Data Structure for solving problems.

Unit I: FUNDAMENTALS OF DATA STRUCTURES **9 Periods**
Introduction-Abstract Data Type (ADT)-Need for Data structures-Types-Operations-Multi Dimensional Arrays-Linked List Types Singly Linked List, Doubly Linked List, Circularly Linked List Operations and Implementation-Reversing a Linked List-Cloning a Linked List-Sorting a Linked List-Applications of Linked Lists-Polynomial Addition-Sparse Matrices.
Unit II: STACKS AND QUEUES **9 Periods**
Stack ADT-Representation and Operations-Implementation-Applications-Balancing Parenthesis and String Traversal-Queue ADT-Representation and Operations-Implementation-Types of Queue-Circular Queue-Deque-Priority Queue-Applications-Reversing the Queue using Stack.
Unit III: TREES **9 Periods**
Terminologies-Binary Trees-Tree Traversal-Expression Trees- Binary Heap-Heap Sort-Binary Search Tree-M-way Search Tree-AVL Tree Operations-Rotations-Insertion-Deletion-Applications.
Unit IV: GRAPHS **9 Periods**
Graph: Terminologies-Representation of Graph-Graph Traversal-Topological Sort-Applications of DFS-Bi connectivity-Euler Circuits-Finding Strongly Connected Components-Applications of BFS-Bipartite Graph-Graph Coloring.
Unit V: SEARCHING, SORTING AND HASHING **9 Periods**
Searching-Linear Search-Binary Search-Sorting-Internal Sorting-Insertion Sort-Shell Sort-Bubble Sort-Radix Sort-External Sorting-Simple Algorithm-Multiway Merge-Hashing-Hash Table-Hash Functions-Collision Resolution Techniques-Rehashing.

Course Outcomes (COs)

CO1: Apply the principles of linear data structures for efficient data management in real time applications. (K3)
CO2: Illustrate the use of stack and queue data structure in real time scenario. (K3)
CO3: Apply tree data structures for solving problems. (K3)

CO4: Outline the importance and applications of graph data structure. (K4)
CO5: Demonstrate the concept of sorting, searching and hashing techniques. (K3)

Resources

1. Text Books

1. Mark Allen Weiss, "Data Structures and Algorithm Analysis in C", 2015, Pearson Education.
2. Sharma A.K, "Data Structure Using C", 2011, Pearson Education.
3. Reema Thareja, "Data Structures Using C 2E", 2014, Oxford University Press.

2. Reference Books

1. Venkatesan R and Lovelyn Rose S, "Data Structures", 2015, Wiely India pvt ltd.
2. Ahmad Talha Siddiqui, ShoebAhad Siddiqui, "Data Structure Using C", 2003, CRC Press.

3. E-Resources

1. NPTEL Data Structures and Algorithms:
   `https://nptel.ac.in/courses/106102064/`
2. NPTEL Programming and Data Structures:
   `https://archive.nptel.ac.in/courses/106/106/106106130/`
3. NPTEL Data Structures and Algorithms - Hash Tables and Trees:
   `https://archive.nptel.ac.in/courses/106/106/106106127/`

Industrial Relevance

Data structures form the backbone of modern Electronic Design Automation (EDA) tools, where graph-based algorithms are essential for circuit partitioning, placement, and routing within VLSI design flows. Proficiency in efficient memory management and searching techniques allows engineers to optimize the performance of embedded firmware and signal processing algorithms running on high-speed hardware. By bridging academic theory with these computational requirements, this course equips students to develop scalable solutions for the semiconductor industry, ensuring reliability and resource optimization in complex hardware systems.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	3	2	0	0	1	0	1	2	3	3	2	2
CO2	3	3	3	2	0	0	1	0	2	1	3	3	2	2
CO3	3	3	3	2	0	0	1	0	2	1	3	3	3	2
CO4	3	2	2	1	0	0	1	0	1	2	3	3	3	2
CO5	3	3	3	3	0	0	1	0	2	1	3	3	3	2
Weighted Average	3.00	2.80	2.80	2.00	0.00	0.00	1.00	0.00	1.60	1.40	3.00	3.00	2.60	2.00

Course Code: U23EVT31
Course Title: Digital System Design
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Electric Circuits and Electron Devices, Linear Algebra and Calculus
SDG: 9

Course Overview

This course provides a comprehensive foundation in digital system design principles essential for modern electronic and VLSI systems. The curriculum encompasses Boolean algebra, combinational and sequential circuit design, finite state machine development, and standard RTL modeling. Students acquire the technical proficiency required for digital hardware design, FPGA implementation, and advanced VLSI system development.

Course Objectives

1. Apply Boolean algebraic postulates and logic minimization techniques for efficient digital circuit realization.
2. Design and analyze complex combinational and sequential digital systems using standard industry methodologies.
3. Develop finite state machine-based controllers and model, simulate, and verify digital systems using RTL design techniques.

Unit I: Boolean Algebra and Logic Minimization **9 Hours**
Boolean postulates-theorems-De Morgan's laws-canonical forms-minterms-maxterms - Sum of Products-Product of Sums-Karnaugh Map minimization-don't care conditions-multi-level logic realization.
Active Learning Activity: Conduct a flipped classroom session where students derive optimized logic circuits using Karnaugh Maps and validate their solutions through simulation using open-source schematic tools.

Unit II: Combinational Logic Circuits **9 Hours**
Half adder-full adder-half subtractor-full subtractor-binary parallel adder-carry look-ahead adder-multiplexers-demultiplexers-encoders-decoders-magnitude comparators-Arithmetic Logic Unit (ALU) design.
Active Learning Activity: Perform simulation-based analysis of arithmetic and data-routing circuits to evaluate functionality and propagation delay using standard open-source simulation environments.

Unit III: Sequential Logic Circuits **9 Hours**
Latches-flip-flops-SR-JK-D-T-flip-flop characteristics-conversions-registers-shift registers-ripple counters-synchronous counter design-ring counters-Johnson counters.
Active Learning Activity: Design and simulate synchronous and asynchronous counters to analyze timing behavior and state transitions in a virtual lab environment.

Unit IV: Finite State Machine Design **9 Hours**
Moore and Mealy FSMs – state diagrams and state tables – state reduction and state assignment

– ASM charts – sequence detector design – introduction to timing and race considerations.
Active Learning Activity: Develop FSM-based digital controllers using ASM charts and perform peer review of state transitions and output logic within a collaborative workspace.

Unit V: Verilog HDL and RTL Design **9 Hours**
Verilog HDL design flow – module structure and ports – data types and operators – continuous assignments – procedural blocks – combinational RTL modeling – sequential RTL modeling – FSM modeling – testbench development – Simulation, waveform analysis and RTL synthesis concepts.
Active Learning Activity: Develop, simulate, and verify Verilog HDL models for combinational, sequential, and FSM-based digital systems using open-source synthesis utilities and waveform analysis.

Course Outcomes (COs)

CO1: Apply Boolean algebra and logic minimization techniques to simplify digital circuits. (K3)
CO2: Design and analyze combinational logic circuits for digital applications. (K3)
CO3: Design sequential circuits using flip-flops, registers, and counters. (K3)
CO4: Analyze and design finite state machine-based digital systems using ASM charts. (K4)
CO5: Develop, simulate, and verify digital circuits using Verilog HDL and RTL design methodologies. (K3)

Resources

1. Text Books

1. Mano, M. M., & Ciletti, M. D. (2020). Digital design: With an introduction to the Verilog HDL, VHDL, and SystemVerilog (6th ed.). Pearson.
2. Roth, C. H., Kinney, L. L., & John, E. B. (2020). Fundamentals of logic design (8th ed.). Cengage Learning.
3. Brown, S., & Vranesic, Z. (2023). Fundamentals of digital logic with Verilog design (4th ed.). McGraw-Hill.
4. Wakerly, J. F. (2021). Digital design: Principles and practices (5th ed.). Pearson Education.
5. Palnitkar, S. (2020). Verilog HDL: A guide to digital design and synthesis (2nd ed.). Pearson.

2. Reference Books

1. Jain, R. P., & Sarawadekar, K. (2022). Modern digital electronics (5th ed.). McGraw-Hill Education.
2. Floyd, T. L. (2023). Digital fundamentals (12th ed.). Pearson Education.
3. Vahid, F. (2020). Digital design with RTL design, VHDL, and Verilog (3rd ed.). Wiley.
4. Bhasker, J. (2021). A Verilog HDL primer (3rd ed.). Star Galaxy Publishing.
5. Unsalan, C., & Tar, B. (2020). Digital system design with FPGA: Implementation using Verilog and VHDL. Cengage Learning.

3. E-Resources

1. NPTEL Digital Circuits
   `https://nptel.ac.in/courses/108105132`
2. EDA Playground Reference
   `https://www.edaplayground.com`
3. MIT OpenCourseWare Computation Structures
   `https://ocw.mit.edu/courses/6-004-computation-structures-spring-2017/`
4. IEEE Xplore Digital Library
   `https://ieeexplore.ieee.org`
5. Open Source Hardware Association
   `https://www.oshwa.org`

Industrial Relevance

This course bridges the gap between digital electronics fundamentals and modern semiconductor design practices. Students acquire essential competencies in digital logic design, finite state machine development, RTL modeling, and functional verification, which form the foundation of FPGA, ASIC, and System-on-Chip (SoC) design flows. The course prepares graduates for careers in semiconductor product development, embedded systems, hardware verification, and VLSI design engineering by aligning theoretical knowledge with contemporary global hardware industry standards.

CO-PO-PSO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	1	-	-	-	-	-	-	-	1	3	1	1
CO2	3	2	2	1	1	-	-	-	-	-	1	3	2	1
CO3	3	2	2	1	1	-	-	-	-	-	1	3	2	1
CO4	3	3	3	2	2	-	-	-	-	-	1	3	3	2
CO5	3	3	3	3	3	1	1	1	1	1	2	3	3	3
Weighted Average	3.00	2.40	2.20	1.75	1.75	1.00	1.00	1.00	1.00	1.00	1.20	3.00	2.20	1.60

Course Code: U23EVT01
Course Title: Analog and Digital Communication
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Linear Algebra and Calculus
SDG: 9,11

Course Overview

This course provides a comprehensive foundation in the principles of analog and digital communication, covering essential modulation, multiplexing, and coding techniques. Students will explore the transition from continuous-wave signaling to robust digital data transmission, emphasizing performance metrics like bandwidth efficiency and error probability. The curriculum bridges theoretical signal analysis with modern hardware implementation requirements, preparing students for the complexities of high-speed data systems.

Course Objectives

1. To understand the fundamentals of analog communication systems and modulation techniques.
2. To analyze digital communication techniques and system performance in the presence of noise.
3. To evaluate source coding and error control coding techniques for reliable data transmission.

Unit I: Introduction to Analog Communication **9 Hours**
Elements of communication systems – Signal types and characteristics – Need for modulation – Amplitude Modulation (AM): generation and detection – DSB-SC and SSB modulation – Power and bandwidth considerations – Frequency Modulation (FM): generation and demodulation – Phase Modulation (PM) – Comparison of AM, FM and PM – Radio transmitters and receivers – Noise in analog communication systems.
Active Learning Activity: Simulation-based comparison of AM and FM signals and their bandwidth requirements.

Unit II: Analog Pulse Modulation and Sampling **9 Hours**
Introduction to pulse modulation – Sampling theorem – Aliasing and anti-aliasing concepts – Pulse Amplitude Modulation (PAM) – Pulse Width Modulation (PWM) – Pulse Position Modulation (PPM) – Time Division Multiplexing (TDM) – Frequency Division Multiplexing (FDM) – Quantization and quantization error – Companding techniques – Signal reconstruction – ADC and DAC fundamentals.
Active Learning Activity: Experimental demonstration of sampling theorem and aliasing effects.

Unit III: Digital Communication Basics **9 Hours**
Introduction to digital communication systems – Advantages of digital communication – Pulse Code Modulation (PCM) – Differential PCM (DPCM) – Delta Modulation (DM) – Line coding techniques: NRZ, RZ and Manchester coding – Inter Symbol Interference (ISI) – Eye diagrams – Matched filter detection – Signal-to-Noise Ratio (SNR) – Bit Error Rate (BER) – Regenerative repeaters – Basics of error detection and correction.
Active Learning Activity: Eye diagram analysis under noise and ISI conditions using simulation tools.

Unit IV: Digital Modulation Techniques **9 Hours**

Need for digital modulation – Amplitude Shift Keying (ASK) – Frequency Shift Keying (FSK) – Binary Phase Shift Keying (BPSK) – Quadrature Phase Shift Keying (QPSK) – Quadrature Amplitude Modulation (QAM) – Minimum Shift Keying (MSK) – Gaussian MSK (GMSK) – Constellation diagrams – Coherent and non-coherent detection – Comparison of digital modulation techniques based on bandwidth efficiency, power efficiency and BER performance.

Active Learning Activity: Comparative analysis of digital modulation schemes using constellation diagrams.

Unit V: Source and Error Control Coding **9 Hours**

Need for source coding – Information content and entropy – Shannon source coding theorem – Huffman coding – Lossless compression basics – Need for error control coding – Error types in communication channels – Parity check – Checksum – Cyclic Redundancy Check (CRC) – Linear block codes – Hamming codes – Introduction to convolutional codes – Performance of coded communication systems.

Active Learning Activity: Implementation of Hamming code encoder and decoder for error detection and correction.

Course Outcomes (COs)

1. Explain the fundamentals of communication systems and analog modulation techniques such as AM, FM and PM. (K2)
2. Apply sampling, pulse modulation, multiplexing, ADC and DAC concepts in communication systems. (K3)
3. Analyze PCM, DPCM, Delta Modulation, line coding techniques and digital communication system performance. (K4)
4. Compare and analyze digital modulation schemes such as ASK, FSK, PSK and QAM based on bandwidth, power and noise performance. (K4)
5. Analyze source coding and error control coding techniques including Huffman coding, CRC, Hamming codes and convolutional codes used in reliable digital communication systems. (K4)

Resources

1. Text Books

1. Haykin, S., & Moher, M. (2022). *Communication systems* (5th ed.). Wiley.
2. Sklar, B. (2020). *Digital communications: Fundamentals and applications* (3rd ed.). Pearson.
3. Proakis, J. G., & Salehi, M. (2021). *Digital communications* (5th ed.). McGraw-Hill.
4. Lathi, B. P., & Ding, Z. (2019). *Modern digital and analog communication systems* (5th ed.). Oxford University Press.
5. Rappaport, T. S. (2023). *Wireless communications: Principles and practice* (2nd ed.). Pearson.

2. Reference Books

1. Taub, H., & Schilling, D. (2021). *Principles of communication systems.* McGraw-Hill.
2. Couch, L. W. (2020). *Digital and analog communication systems* (9th ed.). Pearson.
3. Goldsmith, A. (2022). *Wireless communications.* Cambridge University Press.

4. Tse, D., & Viswanath, P. (2021). *Fundamentals of wireless communication*. Cambridge University Press.

5. Carlson, A. B., & Crilly, P. B. (2020). *Communication systems: An introduction to signals and noise in electrical communication*. McGraw-Hill.

3. E-Resources

1. MIT OpenCourseWare - Signals and Systems:
`https://ocw.mit.edu/courses/res-6-007-signals-and-systems-spring-2011/`
2. NPTEL - Principles of Communication Systems:
`https://nptel.ac.in/courses/108104098`
3. GNU Radio Project Documentation:
`https://wiki.gnuradio.org/`
4. MathWorks Communication Systems Toolbox Documentation:
`https://www.mathworks.com/help/comm/`
5. IEEE Xplore Digital Library - Tutorials on Digital Modulation:
`https://ieeexplore.ieee.org/`

Industrial Relevance

This course serves as a critical bridge between signal theory and semiconductor hardware implementation by providing the mathematical framework for modern digital signal processing (DSP) and ASIC/FPGA transceiver designs. By mastering concepts like eye diagrams, constellation analysis, and error correction coding, students gain the technical proficiency required to design robust communication interfaces, SerDes (Serializer/Deserializer) blocks, and high-speed data interconnects essential in current telecommunications, IoT, and high-performance computing hardware industries.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	1	1	1	-	-	1	-	2	2	1	1
CO2	3	2	2	2	2	1	-	-	1	-	2	3	2	2
CO3	3	3	2	2	3	1	-	-	1	-	2	3	2	2
CO4	3	3	3	3	3	1	-	-	1	-	2	3	2	2
CO5	2	2	2	2	2	1	-	-	1	-	2	2	1	2
Weighted Avg	2.80	2.40	2.00	2.00	2.20	1.00	-	-	1.00	-	2.00	2.60	1.60	1.80

Course Code: U23EVT02
Course Title: Electronic Devices and Circuits
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Electric Circuits and Electron Devices
SDG: 7,9

Course Overview

This course provides a foundational understanding of semiconductor device physics and the operational characteristics of MOSFETs critical for modern VLSI systems. It explores the analysis of analog and digital electronic circuits, emphasizing circuit modeling and performance evaluation techniques. The curriculum bridges device-level physics with practical circuit design, essential for developing robust integrated circuit architectures.

Course Objectives

1. To understand the operation and characteristics of semiconductor devices with emphasis on MOSFETs used in modern VLSI systems.
2. To analyze analog and digital electronic circuits using MOSFET device models and simulation tools.
3. To develop the ability to evaluate the performance of CMOS circuits and analog building blocks used in integrated circuit design.

Unit I: Introduction to Semiconductor Devices for VLSI **9 Hours**
Role of electronic devices in VLSI systems - Review of p-n junction diode for on-chip applications - Zener and Schottky diodes in IC design - MOS capacitor fundamentals - Surface potential, threshold voltage and body effect - MOSFET overview and device scaling - Moore's law and scaling challenges - Introduction to short-channel effects: subthreshold conduction, channel length modulation and DIBL - Importance of MOSFETs in digital and analog ICs.
Active Learning Activity: Flipped classroom and MOS capacitor simulation study.
Unit II: MOSFET Operation and Modelling **9 Hours**
MOSFET structure and types: enhancement and depletion mode devices - Regions of operation: cut-off, triode and saturation - I-V and transfer characteristics - Threshold voltage control through body bias - DC biasing techniques - Small-signal MOSFET model: gm, ro - MOS capacitances (Cgs, Cgd, Cdb) - High-frequency MOSFET model - Short-channel effects and modelling impact - Layout considerations: W/L ratio, parasitics and latch-up.
Active Learning Activity: SPICE simulation and extraction of device parameters.
Unit III: MOSFET-Based Amplifiers and Analog Building Blocks **9 Hours**
Common Source, Common Gate and Common Drain amplifiers - Voltage gain, input/output resistance and bandwidth - Common Source amplifier with active load - Differential amplifier with current mirror load - Current mirrors and source followers - Cascoding concepts - Biasing circuits for analog VLSI - Introduction to CMOS operational amplifiers - Amplifier performance metrics: gain, bandwidth, PSRR and CMRR.
Active Learning Activity: Design and simulation of a differential amplifier.
Unit IV: Switching Behaviour and CMOS Digital Circuits **9 Hours**
MOSFET as a switch - CMOS inverter: voltage transfer characteristics and noise margins - Dynamic behaviour of CMOS inverter - Propagation delay and power dissipation - Rise and fall times - Effect of capacitive loading - CMOS NAND and NOR gates - Transmission gate

and pass-transistor logic - Static and dynamic CMOS logic - Domino logic concepts - Transistor sizing for delay and power optimization - Process variation effects - Introduction to standard-cell based design.
Active Learning Activity: Seminar on CMOS inverter sizing and delay optimization.
Unit V: Oscillators, Voltage References and Layout-Aware Design 9 Hours
Ring oscillator and current-starved ring oscillator - Frequency dependence on stage count - Introduction to PLL applications - Bandgap reference fundamentals - Low Drop-Out (LDO) regulator basics - Layout effects in analog ICs: matching, common-centroid layout and guard rings - Parasitic-aware circuit design - Noise sources in integrated circuits - Layout shielding techniques.
Active Learning Activity: Simulation and analysis of a ring oscillator.

Course Outcomes

CO1: Explain the structure and operation of semiconductor devices used in VLSI circuits and the impact of device scaling. (K2)
CO2: Apply MOSFET models and simulation tools to interpret device characteristics under different operating conditions. (K3)
CO3: Analyze the performance of MOSFET amplifiers and analog building blocks used in integrated circuits. (K4)
CO4: Analyze switching characteristics, delay and power consumption of CMOS digital circuits. (K4)
CO5: Analyze the operation of oscillators, voltage reference circuits and layout-aware analog building blocks used in VLSI systems. (K4)

Resources

1. Text Books

1. Weste, N. H. E., & Harris, D. (2024). *CMOS VLSI design: A circuits and systems perspective* (4th ed.). Pearson.
2. Razavi, B. (2023). *Design of analog CMOS integrated circuits* (2nd ed.). McGraw-Hill Education.
3. Baker, R. J. (2022). *CMOS: Circuit design, layout, and simulation* (4th ed.). Wiley.
4. Kang, S., & Leblebici, Y. (2021). *CMOS digital integrated circuits: Analysis and design* (4th ed.). McGraw-Hill.
5. Rabaey, J. M., Chandrakasan, A., & Nikolic, B. (2020). *Digital integrated circuits: A design perspective* (2nd ed.). Pearson.

2. Reference Books

1. Sedra, A. S., & Smith, K. C. (2020). *Microelectronic circuits* (8th ed.). Oxford University Press.
2. Sze, S. M., & Ng, K. K. (2021). *Physics of semiconductor devices* (4th ed.). Wiley.
3. Johns, D. A., & Martin, K. (2019). *Analog integrated circuit design* (2nd ed.). Wiley.
4. Uyemura, J. P. (2023). *Introduction to VLSI circuits and systems* (2nd ed.). Wiley.
5. Neamen, D. A. (2022). *Semiconductor physics and devices* (5th ed.). McGraw-Hill.

3. E-Resources

1. NPTEL. (n.d.). *Electronic devices and circuits* [Online course]. https://nptel.ac.in/courses/117106127
2. NPTEL. (n.d.). *Analog electronic circuits* [Online course]. https://nptel.ac.in/courses/108106070
3. Falstad, P. (n.d.). *Falstad circuit simulator* [Web application]. https://www.falstad.com/circuit/
4. All About Circuits. (n.d.). *All about circuits: Textbook and tutorials.* https://www.allaboutcircuits.com/
5. Analog Devices. (n.d.). *LTspice* [Computer software]. https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html

Industrial Relevance

This course bridges the gap between fundamental semiconductor physics and the high-performance design requirements of the global semiconductor industry. By focusing on MOSFET scaling, CMOS logic, and layout-aware design, students gain hands-on proficiency in methodologies used by firms like Intel, TSMC, and NVIDIA. Mastering these concepts ensures readiness for advanced roles in ASIC design, standard-cell library development, and analog-mixed signal circuit engineering, aligning academic output with the stringent design-for-manufacturability standards of contemporary IC manufacturing.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	1	-	-	1	1	-	-	-	-	1	1	1	1
CO2	2	2	1	1	3	1	-	1	1	-	2	2	2	2
CO3	3	3	3	2	3	1	-	1	1	1	2	3	2	2
CO4	3	3	3	2	3	1	-	1	1	1	2	3	2	2
CO5	3	3	3	2	3	1	-	1	1	1	2	3	2	2
Weighted Average	2.60	2.40	2.00	1.20	2.60	1.00	-	1.00	1.00	1.00	1.80	2.40	1.80	1.80

Course Code: U23CSP03
Course Title: Data Structures Laboratory
Course Type: Engineering Science Laboratory
L T P C: 0 0 4 2
Total Periods: 60
Prerequisite(s): Problem solving and Programming in C

Course Overview

This laboratory course is designed to provide practical experience in developing and implementing various linear and non-linear data structures for solving computational problems. Students will acquire hands-on skills in selecting, coding, and testing efficient data structures using the C programming language to enhance algorithmic efficiency. These competencies are fundamental for optimizing memory management, signal processing algorithms, and hardware-software interface design within the electronics, communication, and VLSI industries.

Course Objectives

1. To implement various operations on linear and non-linear data structures using standard algorithms.
2. To apply appropriate searching, sorting, and hashing techniques to solve complex data management problems.
3. To analyze and select suitable data structures for specific engineering applications to ensure optimal performance.

Laboratory Experiments

Experiment 1: Practice on Array Operations (CO1)
Experiment 2: Implementation of Singly, Doubly and Circularly Linked List (CO1)
Experiment 3: Implementation of Stack, Queue and its Applications (CO1)
Experiment 4: Operations on Binary Search Tree and AVL tree (CO1)
Experiment 5: Programs on Graph Traversal (CO1)
Experiment 6: Implementation of searching and sorting algorithms (CO2)
Experiment 7: Implementation of Hashing and Collision Resolution Techniques (CO2)
Experiment 8: Mini Project (CO3)

Course Outcomes

CO1: Implement various operations on Linear and Non-Linear Data Structures. (K3)
CO2: Implement Searching, Sorting and Hashing techniques to solve the given problem. (K3)
CO3: Choose suitable Data Structures and solve the given problem. (K3)

Resources

Text Books

1. Mark Allen Weiss, "Data Structures and Algorithm Analysis in C", 2015, Pearson Education.
2. Sharma A K, "Data Structure Using C", 2011, Pearson Education.
3. Reema Thareja, "Data Structures Using C 2E", 2014, Oxford University Press.

Reference Books

1. Venkatesan R, Lovelyn Rose S, "Data Structures" 2015, Wiely India pvt ltd.
2. Ahmad Talha Siddiqui, Shoeb Ahad Siddiqui, "Data Structure Using C", 2003, CRC Press.

E-Resources

`https://dsl-iiith.vlabs.ac.in/List%20of%20experiments.html`
`https://cse01-iiith.vlabs.ac.in/List%20of%20experiments.html`
`https://www.geeksforgeeks.org/data-structures/`
`https://www.programiz.com/dsa`
`https://www.coursera.org/learn/data-structures`

Industrial Relevance

This laboratory fosters essential measurement, instrumentation, and hardware-implementation skills by requiring students to model real-world signals and data as structured entities. Through circuit debugging and validation techniques, students learn to optimize resource allocation, which is critical for semiconductor manufacturing, communication protocol testing, and embedded system design. These skills directly translate to the VLSI industry, where efficient data handling is required to optimize EDA tool performance and hardware architectural synthesis.

CO–PO–PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	3	2	3	-	-	1	1	2	3	2	1	-
CO2	3	3	3	3	3	-	-	1	1	2	3	3	2	-
CO3	3	3	3	3	3	1	1	1	2	2	1	2	3	3
Weighted Average	3.00	2.67	3.00	2.67	3.00	1.00	1.00	1.00	1.33	2.00	2.33	2.33	2.00	3.00

Course Code: U23EVP31
Course Title: Digital System Design Laboratory
Course Type: Professional Core Laboratory
L T P C: 0 0 4 2
Total Periods: 60
Prerequisite(s): Electric Circuits and Electron Devices

Course Overview

This laboratory course provides a hands-on foundation in digital system design principles, bridging the gap between theoretical Boolean logic and modern hardware implementation. Students will develop practical skills in designing, simulating, and verifying combinational and sequential circuits using both discrete components and hardware description languages. The course is essential for preparing students for professional roles in the semiconductor, embedded systems, and VLSI design industries.

Course Objectives

1. Implement and verify combinational and sequential logic circuits using industry-standard simulation and hardware prototyping tools.
2. Design and debug finite state machine-based controllers to solve complex logic sequence requirements.
3. Develop and synthesize digital hardware models using Verilog HDL to gain proficiency in modern RTL design flows.

Laboratory Experiments

Experiment 1: Logic Gate Implementation and Boolean Minimization (CO1)
Design and realize Boolean functions using universal gates and verify truth tables through experimental measurement.
Laboratory Activity: Construct a multi-level logic circuit on a breadboard, verify outputs, and troubleshoot discrepancies between theoretical minimization and hardware behavior.
Experiment 2: Karnaugh Map-based Logic Circuit Optimization (CO1)
Apply K-map techniques to minimize complex switching expressions and implement the optimized circuits using logic ICs.
Laboratory Activity: Derive the minimal gate configuration for a four-variable function, build the circuit, and perform an error analysis compared to the non-minimized version.
Experiment 3: Design of Arithmetic Logic Units (CO2)
Construct and test combinational arithmetic circuits including half adders, full adders, and multi-bit binary adders.
Laboratory Activity: Implement a 4-bit parallel adder, measure propagation delay using an oscilloscope, and verify carry propagation across bit stages.
Experiment 4: Data Routing and Code Conversion Circuits (CO2)
Design and analyze multiplexers, demultiplexers, encoders, and decoders for data routing and display applications.
Laboratory Activity: Integrate a BCD-to-7-segment decoder with a multiplexed display system and evaluate the timing stability of data selection signals.

Experiment 5: Sequential Element Characterization (CO3)
Analyze the characteristics and triggering mechanisms of various latches and flip-flops.
Laboratory Activity: Test the race-around condition in JK flip-flops and design a flip-flop conversion circuit to transform a D flip-flop into a T flip-flop.
Experiment 6: Design of Synchronous and Asynchronous Counters (CO3)
Build and test various counter architectures including ripple, ring, and Johnson counters.
Laboratory Activity: Design a modulus-N counter, observe state transitions on a logic analyzer, and verify timing constraints against the clock frequency.
Experiment 7: Mealy and Moore State Machine Design (CO4)
Develop state diagrams and tables for a sequence detector and implement the FSM using D flip-flops.
Laboratory Activity: Construct the sequential controller on a hardware trainer kit, conduct a state transition validation test, and verify outputs against the state table.
Experiment 8: ASM Chart-based Controller Implementation (CO4)
Translate Algorithmic State Machine (ASM) charts into hardware logic for complex control unit design.
Laboratory Activity: Design a traffic light controller using ASM logic and perform a peer-review verification of state sequence and transition conditions.
Experiment 9: Combinational and Sequential RTL Modeling (CO5)
Develop Verilog HDL models for basic combinational blocks and sequential registers/buffers.
Laboratory Activity: Write behavioral and dataflow descriptions for a 4-bit shifter, perform functional simulation, and analyze the resulting waveforms.
Experiment 10: FSM Synthesis and Verification (CO5)
Model complex FSMs in Verilog and perform comprehensive testbench-based verification.
Laboratory Activity: Create a testbench to inject stimuli into an FSM module, compare synthesized gate-level behavior with RTL simulation results, and debug logic hazards.

Course Outcomes

CO1: Apply Boolean algebra and logic minimization techniques to simplify digital circuits. (K3)
CO2: Design and analyze combinational logic circuits for digital applications. (K3)
CO3: Design sequential circuits using flip-flops, registers, and counters. (K3)
CO4: Analyze and design finite state machine-based digital systems using ASM charts. (K4)
CO5: Develop, simulate, and verify digital circuits using Verilog HDL and RTL design methodologies. (K3)

Resources

Text Books

1. Mano, M. M., & Ciletti, M. D. (2024). *Digital design: With an introduction to the Verilog HDL, VHDL, and System Verilog* (6th ed.). Pearson.

2. Roth, C. H., Kinney, L. L., & John, E. B. (2022). *Fundamentals of logic design* (8th ed.). Cengage Learning.

3. Brown, S., & Vranesic, Z. (2023). *Fundamentals of digital logic with Verilog design* (4th ed.). McGraw-Hill.

4. Wakerly, J. F. (2021). *Digital design: Principles and practices* (5th ed.). Pearson Education.

5. Palnitkar, S. (2020). *Verilog HDL: A guide to digital design and synthesis* (2nd ed.). Pearson.

Reference Books

1. Jain, R. P., & Sarawadekar, K. (2022). *Modern digital electronics* (5th ed.). McGraw-Hill Education.
2. Floyd, T. L. (2023). *Digital fundamentals* (12th ed.). Pearson Education.
3. Vahid, F. (2020). *Digital design with RTL design, VHDL, and Verilog* (3rd ed.). Wiley.
4. Bhasker, J. (2021). *A Verilog HDL primer* (3rd ed.). Star Galaxy Publishing.
5. Unsalan, C., & Tar, B. (2020). *Digital system design with FPGA: Implementation using Verilog and VHDL*. Cengage Learning.

E-Resources

1. `https://nptel.ac.in/courses/108105132`
2. `https://www.edaplayground.com`
3. `https://ocw.mit.edu/courses/6-004-computation-structures-spring-2017/`
4. `https://ieeexplore.ieee.org`
5. `https://www.oshwa.org`

Industrial Relevance

This laboratory course is critical for developing essential competencies in hardware measurement, instrumentation usage, and circuit debugging, which are foundational in the semiconductor and VLSI industries. Through hands-on experiments, students gain expertise in hardware implementation, functional validation, and signal verification using oscilloscopes and logic analyzers. These skills are directly applicable to the development of complex FPGA, ASIC, and SoC systems, ensuring that graduates are prepared for professional careers in hardware design, verification, and embedded system engineering.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	2	0	0	2	2	0	1	3	2	1
CO2	3	2	2	2	2	0	0	2	2	0	1	3	2	1
CO3	3	2	2	2	2	0	0	2	2	0	1	3	2	1
CO4	3	3	3	3	3	0	0	2	2	0	1	3	3	2
CO5	3	3	3	3	3	0	0	2	2	0	2	3	3	3
Weighted Average	3.00	2.40	2.40	2.40	2.40	0.00	0.00	2.00	2.00	0.00	1.20	3.00	2.40	1.60

Course Code: U23EVP01
Course Title: Analog and Digital Communication Lab
Course Type: Professional Core Laboratory
L T P C: 0 0 4 2
Total Hours: 60
SDG: 9,11

Course Overview

This laboratory course provides practical training in the design, simulation, and analysis of analog and digital communication circuits. Students will develop essential skills in signal generation, modulation, multiplexing, and error control coding through advanced computer-aided simulation tools. These competencies are highly relevant for careers in electronics, communication systems, and VLSI design, focusing on system performance validation and signal integrity.

Course Objectives

1. To demonstrate the generation and demodulation of various analog and digital modulation techniques using simulation environments.
2. To analyze the performance of communication systems through software-based signal measurement and spectral analysis.
3. To evaluate data integrity and system reliability using simulation-based error detection/correction coding and multiplexing schemes.

Laboratory Experiments

Experiment 1: Analog Modulation Simulation (AM) (CO1)
Simulate an Amplitude Modulation (AM) system and analyze its spectral characteristics.
Laboratory Activity: Design an AM modulator in a simulation environment, vary the modulation index, and observe the frequency spectrum and time-domain signals to verify bandwidth requirements.
Experiment 2: Angle Modulation Simulation (FM) (CO1)
Simulate a Frequency Modulation (FM) system and perform comparative performance analysis.
Laboratory Activity: Implement an FM modulator, perform a sweep analysis of the carrier signal, and demonstrate the effect of modulation index on bandwidth using simulation-based FFT analysis.
Experiment 3: Sampling and Reconstruction Analysis (CO2)
Simulate the sampling process and investigate the impact of sampling rates on signal reconstruction.
Laboratory Activity: Simulate a continuous-time signal, apply a sampling pulse train, demonstrate aliasing effects when violating the Nyquist criterion, and implement a digital filter for signal reconstruction.
Experiment 4: Multiplexing Technique Simulation (TDM) (CO2)
Model and simulate a Time Division Multiplexing (TDM) system for multi-signal transmission.
Laboratory Activity: Create a simulation block for multi-channel TDM, perform time-interleaving of distinct signals, and simulate the demultiplexing process to retrieve original signal components.
Experiment 5: Pulse Code Modulation (PCM) Simulation (CO3)
Simulate a full PCM chain including quantization and encoding.

Laboratory Activity: Design a simulation model to perform uniform quantization on an analog waveform and implement a digital encoder to observe the resulting pulse code stream.

Experiment 6: Line Coding and ISI Characterization (CO3)

Simulate line coding schemes and evaluate system performance using eye diagrams.

Laboratory Activity: Generate various line codes (NRZ, Manchester), introduce channel noise, and utilize simulation-based eye diagram tools to measure inter-symbol interference and jitter.

Experiment 7: Digital Modulation Simulation (ASK/FSK) (CO4)

Simulate ASK and FSK modulation schemes and analyze their constellation performance.

Laboratory Activity: Develop simulation models for ASK and FSK modulators, visualize the modulated outputs, and analyze the bit error rate (BER) versus signal-to-noise ratio (SNR) curves.

Experiment 8: Phase Shift Keying (BPSK/QPSK) Simulation (CO4)

Simulate high-efficiency digital modulation schemes and assess their performance metrics.

Laboratory Activity: Design a BPSK/QPSK transmission chain in a simulation environment, plot constellation diagrams, and conduct a comparative analysis of power versus bandwidth efficiency.

Experiment 9: Source Coding Efficiency (CO5)

Perform simulation-based source coding analysis using information theory metrics.

Laboratory Activity: Implement an algorithm to compute entropy and generate Huffman code tables for a given data source, evaluating the achievable compression ratio via simulation.

Experiment 10: Error Control Coding Simulation (CRC) (CO5)

Model and test error detection capabilities using simulation tools.

Laboratory Activity: Implement a cyclic redundancy check (CRC) encoder/decoder block in the simulation environment, introduce bit errors into the transmitted stream, and verify successful detection and reporting.

Course Outcomes

CO1: Explain the fundamentals of communication systems and analog modulation techniques such as AM, FM and PM. (K2)

CO2: Apply sampling, pulse modulation, multiplexing, ADC and DAC concepts in communication systems. (K3)

CO3: Analyze PCM, DPCM, Delta Modulation, line coding techniques and digital communication system performance using SNR, BER and eye diagrams. (K4)

CO4: Compare and analyze digital modulation schemes such as ASK, FSK, PSK and QAM based on bandwidth efficiency, power efficiency and BER performance. (K4)

CO5: Apply source coding and error control coding techniques such as Huffman coding, CRC and Hamming codes for reliable digital communication systems. (K3)

Resources

Text Books

1. Proakis, J. G., & Salehi, M. (2021). *Digital communications.* McGraw-Hill.
2. Haykin, S., & Moher, M. (2022). *Communication systems.* Wiley.
3. Lathi, B. P., & Ding, Z. (2019). *Modern digital and analog communication systems.* Oxford University Press.
4. Couch, L. W. (2020). *Digital and analog communication systems.* Pearson.
5. Rappaport, T. S. (2024). *Wireless communications.* Prentice Hall.

Reference Books

1. Sklar, B. (2020). *Digital communications: Fundamentals and applications*. Pearson.
2. Taub, H., Schilling, D. L., & Saha, G. (2023). *Principles of communication systems*. Tata McGraw-Hill.
3. Stallings, W. (2022). *Data and computer communications*. Pearson.
4. Glover, I. A., & Grant, P. M. (2021). *Digital communications*. Routledge.
5. Carlson, A. B., & Crilly, P. B. (2020). *Communication systems*. McGraw-Hill.

E-Resources

1. NPTEL. (n.d.). *Principles of digital communications* [Online course]. `https://nptel.ac.in/courses/108104091`
2. Massachusetts Institute of Technology. (2006). *Principles of digital communications I* [Online course]. MIT OpenCourseWare.urlhttps://ocw.mit.edu/courses/6-450-principles-of-digital-communications-i-fall-2006
3. IEEE Communications Society. (n.d.). *Tutorials* [Web resource]. `https://comsoc.org/publications/tutorials`
4. GNU Radio. (n.d.). *Tutorials* [Web resource]. `https://wiki.gnuradio.org/index.php/Tutorials`
5. MathWorks. (n.d.). *Communications toolbox documentation* [Computer software manual]. `https://in.mathworks.com/help/comm/index.html`

Industrial Relevance

This laboratory course is foundational for developing proficiency in measurement and simulation, critical for the semiconductor and embedded systems sectors. Students gain essential hands-on skills in digital signal simulation, system testing, and performance debugging, which are vital for characterizing RF front-ends, high-speed SerDes, and SoC interfaces. These practical competencies ensure that graduates can perform rigorous validation and verification of communication protocols in modern VLSI and telecommunications industries.

CO–PO–PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	1	1	3	3	1	-	2	2	1	1	3	2	1
CO2	3	2	2	3	3	1	-	2	2	1	1	3	2	1
CO3	3	3	2	3	3	1	-	2	2	1	2	3	2	2
CO4	3	3	2	3	3	1	-	2	2	1	2	3	2	2
CO5	3	2	2	3	3	1	-	2	2	1	2	3	2	2
Weighted Average	2.80	2.20	1.80	3.00	3.00	1.00	-	2.00	2.00	1.00	1.60	3.00	2.00	1.60

Course Code: U23EVP02
Course Title: Electronic Devices and Circuits Laboratory
Course Type: Professional Core Laboratory
L T P C: 0 0 4 2
Total Hours: 30
SDG: 7,9

Course Overview

The purpose of this laboratory course is to provide students with hands-on experience in simulating, analyzing, and validating basic electronic circuits using open-source academic simulation tools and standard testing methodologies. Through project-based and activity-driven learning, students develop practical skills in circuit debugging, waveform analysis, and parameter extraction for fundamental semiconductor devices including diodes, MOSFETs, amplifiers, and oscillators. This course directly bridges core electronic theories with practical implementation, fostering the design thinking and verification proficiencies required in the modern electronics, communication, embedded systems, and VLSI industries.

Course Objectives

1. To simulate, test, and analyze the switching and DC characteristics of semiconductor diode circuits, including rectifiers, clippers, and clampers, using EDA software.
2. To extract critical device parameters (g_m, V_{th}) of MOSFETs and evaluate the transient performance and propagation delay of CMOS building blocks.
3. To design, construct, and evaluate the frequency response, gain, and biasing conditions of multi-stage amplifiers, differential amplifiers, and feedback oscillators suitable for VLSI subsystems.

Laboratory Experiments

Experiment 1: Simulation and analysis of Half-wave and Full-wave Rectifier circuits (CO1)
Exact experiment statement: Simulate and analyze the half-wave and full-wave rectifier circuits with and without capacitive filtering to evaluate ripple factor, peak inverse voltage, and rectification efficiency.
Laboratory Activity: Construct the rectifier circuits using open-source simulation tools, measure the input and output time-domain waveforms, calculate the numerical ripple factor for varying load capacitances, and verify circuit behavior against theoretical expectations.

Experiment 2: Design and simulation of Diode Clipper and Clamper circuits (CO1)
Exact experiment statement: Design and simulate positive, negative, and biased diode clipper and clamper circuits to observe wave-shaping and DC voltage shifting capabilities.
Laboratory Activity: Implement series and parallel clipper topologies as well as positive/negative clamper networks using virtual instrumentation; troubleshoot waveform distortion and measure clipping thresholds and DC shift levels across different input sinusoidal amplitudes.

Experiment 3: Plotting MOSFET I-V characteristics and extracting gm, Vth (CO2)
Exact experiment statement: Plot the drain ($I_D - V_{DS}$) and transfer ($I_D - V_{GS}$) characteristics of an N-channel MOSFET and extract its transconductance (g_m) and threshold voltage (V_{th}).
Laboratory Activity: Perform DC sweep simulations on an NMOS device using an academic

simulator; extract the slope of the transfer curve in the saturation region to determine transconductance (g_m) and intercept the voltage axis to identify the threshold voltage (V_{th}).

Experiment 4: Design and transient analysis of CMOS Inverter with delay measurement (CO2)
Exact experiment statement: Design a standard CMOS inverter, perform transient simulation, and measure propagation delay (t_{pHL}, t_{pLH}) and rise/fall times across various capacitive loads.
Laboratory Activity: Build a complementary MOSFET inverter network; apply pulse input excitation, perform transient time-domain analysis, utilize measurement cursors to log switching delays at 50% voltage thresholds, and evaluate load-dependent performance degradation.

Experiment 5: Simulation of Common Source Amplifier with biasing circuit (CO3)
Exact experiment statement: Simulate an NMOS Common Source (CS) amplifier with voltage divider biasing and evaluate its small-signal voltage gain, input impedance, and frequency response.
Laboratory Activity: Design the biasing network to establish a stable Q-point in saturation; perform AC small-signal analysis to generate Bode plots, measure mid-band voltage gain, and identify the lower and upper 3-dB cut-off frequencies.

Experiment 6: Simulation of Differential Amplifier with Current Mirror Load (CO3)
Exact experiment statement: Simulate a MOSFET differential amplifier utilizing an active current mirror load to analyze differential-mode gain, common-mode gain, and Common Mode Rejection Ratio (CMRR).
Laboratory Activity: Construct the active-loaded differential pair; apply differential and common-mode test signals independently, measure output voltage swings, compute the CMRR in decibels, and analyze the biasing stability provided by the active load.

Experiment 7: Implementation and analysis of negative feedback amplifier circuit (CO4)
Exact experiment statement: Implement a negative feedback amplifier topology (voltage-series or current-series) and analyze its effect on gain stability, bandwidth extension, and distortion reduction.
Laboratory Activity: Simulate an amplifier stage both open-loop and closed-loop; measure and tabulate the changes in mid-band gain and upper cut-off frequency to experimentally verify the gain-bandwidth product conservation principle.

Experiment 8: Performance comparison of amplifiers with and without feedback (CO4)
Exact experiment statement: Conduct a comprehensive performance comparison of amplifier configurations with and without negative feedback by evaluating input/output impedance and harmonic distortion metrics.
Laboratory Activity: Perform Fourier analysis within the simulation tool to measure Total Harmonic Distortion (THD) and utilize AC test current injection methods to calculate input and output impedance values for both open-loop and feedback-stabilized conditions.

Experiment 9: Design and simulation of RC Phase Shift Oscillator (CO5)
Exact experiment statement: Design and simulate an RC phase-shift oscillator using an active amplifying stage to generate a sustained sinusoidal waveform at a specified oscillation frequency.
Laboratory Activity: Calculate feedback resistor and capacitor values to satisfy the Barkhausen stability criterion for 180-degree phase shift; simulate the transient startup behavior, observe loop gain conditions for sustained oscillations, and measure the output frequency.

Experiment 10: Ring Oscillator design with delay analysis using CMOS inverter

chain (CO5)
Exact experiment statement: Design an odd-stage CMOS ring oscillator, perform transient simulation, and analyze the oscillation frequency to extract the average stage propagation delay.
Laboratory Activity: Implement a 5-stage or 7-stage cascaded CMOS inverter loop; simulate self-sustained oscillations, measure the fundamental output period using time cursors, and calculate the individual gate delay applicable to VLSI clock generation circuits.

Course Outcomes

Upon completion of this laboratory course, the students will be able to:

CO1: Interpret the behavior of diode-based circuits such as rectifiers, clippers, and clampers using simulation tools. (Bloom's Level: Understand - K2)

CO2: Simulate and measure the DC and switching characteristics of MOSFETs and CMOS inverters using EDA tools. (Bloom's Level: Apply - K3)

CO3: Analyze the gain and biasing conditions of small-signal MOSFET amplifiers and differential amplifiers. (Bloom's Level: Analyze - K4)

CO4: Evaluate the performance of amplifiers with and without negative feedback through simulation and performance metrics. (Bloom's Level: Evaluate - K5)

CO5: Design and simulate basic analog building blocks such as oscillators and ring oscillators for VLSI applications. (Bloom's Level: Create - K6)

Resources

Text Books

1. Sedra, A. S., & Smith, K. C. (2020). *Microelectronic circuits* (8th ed.). Oxford University Press.

2. Neamen, D. A. (2021). *Microelectronics: Circuit analysis and design* (5th ed.). McGraw Hill Education.

3. Rashid, M. H. (2019). *Microelectronic circuits: Analysis and design* (3rd ed.). Cengage Learning.

4. Boylestad, R. L., & Nashelsky, L. (2023). *Electronic devices and circuit theory* (12th ed.). Pearson Education.

5. Millman, J., Halkias, C. C., & Parikh, C. (2021). *Integrated electronics: Analog and digital circuits and systems* (3rd ed.). McGraw Hill Education.

Reference Books

1. Razavi, B. (2021). *Fundamentals of microelectronics* (3rd ed.). John Wiley & Sons.

2. Jaeger, R. C., & Blalock, T. N. (2022). *Microelectronic circuit design* (6th ed.). McGraw Hill Education.

3. Baker, R. J. (2019). *CMOS: Circuit design, layout, and simulation* (4th ed.). IEEE Press / Wiley.

4. Malvino, A. P., & Bates, D. J. (2020). *Electronic principles* (9th ed.). McGraw Hill Education.

5. Streetman, B. G., & Banerjee, S. K. (2020). *Solid state electronic devices* (8th ed.). Pearson Education.

E-Resources

1. NPTEL. (n.d.). *Electronic devices and circuits.* `https://nptel.ac.in/courses/117106127`

2. NPTEL. (n.d.). *Analog electronic circuits.* `https://nptel.ac.in/courses/108106070`

3. Analog Devices. (n.d.). *LTspice simulation tool.* `https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html`

4. Falstad. (n.d.). *Online circuit simulator.* `https://www.falstad.com/circuit/`

5. All About Circuits. (n.d.). *Textbooks, tutorials, and tools.* `https://www.allaboutcircuits.com/`

Industrial Relevance

This laboratory course is exceptionally relevant to the modern electronics, semiconductor, communication, embedded systems, and VLSI industries as it systematically instills critical measurement, instrumentation, and hardware implementation skills. By utilizing electronic design automation (EDA) software to simulate diode shaping networks, MOSFET characterization curves, and CMOS delay architectures, students acquire rigorous circuit debugging and communication system testing capabilities essential for physical design and chip verification. Furthermore, practical hands-on activities involving differential gain extraction, feedback stability evaluation, and ring oscillator timing validation mirror industry-standard validation and verification techniques. Mastery of these practical domain competencies prepares graduates to effectively analyze timing failures, troubleshoot signal integrity anomalies, and optimize analog building blocks within advanced ASIC, FPGA, and embedded system design flows.

CO–PO–PSO Articulation Matrix

CO / PO-PSO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	–	2	–	–	–	–	–	–	–	3	2	1
CO2	3	2	2	2	3	–	–	–	–	–	–	3	3	2
CO3	3	3	3	2	3	–	–	–	–	1	–	3	2	2
CO4	2	3	3	3	3	–	–	–	–	2	–	2	3	3
CO5	3	3	3	3	3	–	–	–	1	2	1	3	3	3
Weighted Average	2.80	2.60	2.75	2.40	3.00	–	–	–	1.00	1.67	1.00	2.80	2.60	2.20

Course Code: U23ECT10
Course Title: Linear Integrated Circuits
Course Type: Professional Core
L T P C: 3 0 0 3
Total Periods : 45
Prerequisites: Electric Circuits and Electron Devices

Course Overview

This course provides a comprehensive study of the fundamental building blocks and operational characteristics of linear integrated circuits. Students will explore the diverse linear and non-linear applications of operational amplifiers, including signal conditioning, filtering, and precision data conversion techniques. Furthermore, the curriculum covers essential analog signal processing components such as analog multipliers, phase-locked loops, and specialized waveform generation ICs.

Course Objectives

1. To introduce the basic building blocks of linear integrated circuits.
2. To learn the linear and non-linear applications of operational amplifiers.
3. To learn the theory of ADC and DAC, along with analog multipliers, PLL, and special function ICs.

Unit I: BASICS OF OPERATIONAL AMPLIFIERS 9 Periods
Current mirror and current sources-Current sources as active loads-Voltage sources-Voltage References-BJT Differential amplifier with active loads-Basic information about op-amps- Operational Amplifier General operational amplifier stages-Ideal-DC and AC performance characteristics, slew rate, Open and closed loop configurations.
Unit II: APPLICATIONS OF OPERATIONAL AMPLIFIERS 9 Periods
Sign Changer-Scale Changer-Inverting and non-inverting amplifier-Voltage Follower-V-to-I and I-to-V converters-adder, subtractor, Instrumentation amplifier-Integrator, Differentiator, Logarithmic amplifier, Antilogarithmic amplifier-Comparators, Schmitt trigger, Precision rectifier, peak detector, clipper and clamper-Low-pass, high-pass and band-pass Butterworth filters.
Unit III: ANALOG MULTIPLIER AND PLL 9 Periods
Variable transconductance technique-Analog Multiplier using Emitter Coupled Transistor Pair Gilbert Multiplier cell-analog multiplier ICs and their applications-Operation of the basic PLL-Closed loop analysis-Voltage controlled oscillator-Monolithic PLL IC 565-application of PLL for AM detection, FM detection, FSK demodulation and Frequency synthesizer.
Unit IV: ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS 9 Periods
Analog and Digital Data Conversions-D/A converter weighted resistor type-R-2R Ladder type-Voltage Mode and Current-Mode R2R Ladder types switches for D/A converters-high speed sample-and-hold circuits-A/D Converters Flash type-Successive Approximation type-Single Slope type-Dual Slope type A/D Converter using Voltage-to-Time Conversion.
Unit V: WAVEFORM GENERATORS AND SPECIAL FUNCTION ICS 9 Periods
Sine-wave generators-Multivibrators and Triangular wave generator-Saw-tooth wave generator-ICL8038 function generator-Timer IC 555-Astable and monstable-IC Voltage regulators-Three terminal fixed and adjustable voltage regulators-IC 723 general purpose regulator-Monolithic

switching regulator, Frequency to Voltage and Voltage to Frequency converters, Audio Power amplifier, Video Amplifier, Isolation Amplifier.

Course Outcomes (COs)

CO1: Infer DC characteristics, AC characteristics of operational amplifiers. (K2)
CO2: Make use of operational amplifiers in various applications. (K3)
CO3: Develop the analog multiplier and PLL using integrated circuits. (K3)
CO4: Construct ADC and DAC using operational amplifiers. (K3)
CO5: Analyze special function ICs and waveform Generators using operational amplifiers circuits. (K4)

Resources

1. Text Books

1. Roy Choudhry D., Shail Jain, "Linear Integrated Circuits", 5th edition 2018, New Age International Pvt. Ltd.

2. Sergio Franco, "Design with Operational Amplifiers and Analog Integrated Circuits", 4th Edition, 2016, Tata McGraw-Hill, (Unit I - V).

2. Reference Books

1. Ramakant A. Gayakwad, "OP-AMP and Linear ICs", 4th Edition, 2015, Prentice Hall / Pearson Education.

2. Robert F. Coughlin, Frederick F. Driscoll, "Operational Amplifiers and Linear Integrated Circuits", Sixth Edition, 2001, PHI.

3. Salivahanan S. and Kanchana Bhaskaran V.S, "Linear Integrated Circuits", 2nd Edition, 4th Reprint, 2016, TMH.

4. Gray and Meyer, "Analysis and Design of Analog Integrated Circuits", 2005, Wiley International.

5. William Stanley D, "Operational Amplifiers with Linear Integrated Circuits", 2004, Pearson Education.

3. E-Resources

1. NPTEL Linear Integrated Circuits Course Overview
   `https://nptel.ac.in/courses/108108111`

2. NPTEL Analog IC Design Fundamentals
   `https://nptel.ac.in/courses/117107094`

3. NPTEL Advanced Linear Integrated Circuits
   `https://onlinecourses.nptel.ac.in/noc24ee73/preview`

4. IEEE Solid-State Circuits Society Educational Resources
   `https://sscs.ieee.org/`

5. Analog Devices Educational Library on Operational Amplifiers
   `https://www.analog.com/en/education.html`

Industrial Relevance

This course bridges academic theory and industrial practice by providing the foundational knowledge required for modern semiconductor and hardware design. By mastering operational amplifiers, data converters, and signal processing ICs, students gain the competency to design precision analog interfaces, sensor conditioning circuits, and frequency synthesizers essential in current VLSI and communication system deployments.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	3	3	2	1	0	0	0	1	2	3	3	2
CO2	3	3	3	3	2	1	0	0	0	1	2	3	3	2
CO3	3	3	3	3	2	1	0	0	0	1	2	3	3	2
CO4	3	3	3	3	2	1	0	0	0	1	2	3	3	2
CO5	3	3	3	3	2	1	0	0	0	1	2	3	3	2
Weighted Average	3.00	3.00	3.00	3.00	2.00	1.00	0.00	0.00	0.00	1.00	2.00	3.00	3.00	2.00

Course Code: U23EVT03
Course Title: Electro Magnetic Fields and Transmission lines
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
Prerequisite(s): Linear Algebra and Calculus, Engineering Physics
SDG: 7,9

Course Overview

This course provides a comprehensive exploration of electromagnetic fields, covering static and time-varying phenomena essential for understanding high-frequency electronic behavior. Students will examine the fundamental principles of electrostatics and magnetostatics before advancing to Maxwell's equations and wave propagation mechanisms. The curriculum emphasizes the application of these theories to transmission line analysis, ensuring a robust foundation for modern hardware design and signal integrity studies.

Course Objectives

1. To analyze electric and magnetic field distributions using vector calculus and fundamental laws for static and time-varying conditions.
2. To derive and interpret Maxwell's equations to explain the propagation of electromagnetic waves in various media.
3. To evaluate transmission line performance using impedance matching techniques and reflection analysis to ensure efficient signal transfer.

Unit I: Vector Analysis and Coordinate Systems **9 Hours**
Vector algebra fundamentals-Coordinate systems: Cartesian, Cylindrical, and Spherical-Differential elements-Gradient of a scalar field-Divergence of a vector field-Curl of a vector field-Divergence theorem-Stokes' theorem-Physical interpretation of vector operators and coordinate transformations.
Active Learning Activity: Simulation-based Lab: Visualizing vector fields using open-source numerical computing environments.
Unit II: Electrostatics **9 Hours**
Coulomb's law-Electric field intensity-Electric field due to various charge distributions-Electric flux density-Gauss's law and its applications-Electric potential-Relationship between electric field and potential-Energy stored in electrostatic fields-Boundary conditions-Poisson's and Laplace's equations.
Active Learning Activity: Flipped Classroom: Analysis of capacitance configurations using field solver conceptual models.
Unit III: Magnetostatics **9 Hours**
Biot-Savart law-Ampere's circuital law-Magnetic field due to current elements-Magnetic flux density-Magnetic scalar and vector potentials-Boundary conditions for magnetic fields-Magnetic forces-Magnetic dipole-Magnetization and permeability-Inductance and mutual inductance- Energy stored in magnetic fields.
Active Learning Activity: Simulation-based Lab: Modeling magnetic flux density in high-inductance circuit components.
Unit IV: Time-Varying Fields and Maxwell's Equations **9 Hours**
Faraday's law of electromagnetic induction-Displacement current-Maxwell's equations in point form-Maxwell's equations in integral form-Constitutive relations-Wave equations-Electromagnetic

wave propagation in free space-Uniform plane waves-Poynting theorem-Time-harmonic fields.
Active Learning Activity: Flipped Classroom: Deriving wave propagation characteristics in conductive and dielectric media.

Unit V: Transmission Lines **9 Hours**

Transmission line equations-Characteristic impedance-Propagation constant-Lossless and lossy lines-Reflection coefficient-VSWR-Impedance matching-Smith chart and its applications-Quarter-wave and half-wave transformers-Transmission line applications in communication systems.
Active Learning Activity: Simulation-based Lab: Smith chart implementation for impedance matching in high-speed interconnect design.

Course Outcomes (COs)

CO1: Apply vector calculus to solve complex electromagnetic field problems in diverse coordinate systems. (K3)
CO2: Analyze electrostatic field distributions and capacitive energy storage in multi-dielectric configurations. (K4)
CO3: Evaluate magnetic field intensity and inductance for various current-carrying geometries. (K4)
CO4: Formulate Maxwell's equations to characterize time-varying field propagation and energy flow. (K3)
CO5: Design impedance matching networks for transmission lines to minimize signal reflections. (K4)

Resources

1. Text Books

1. Sadiku, M. N. O. (2021). Elements of Electromagnetics (7th ed.). Oxford University Press.
2. Cheng, D. K. (2020). Field and Wave Electromagnetics (2nd ed.). Pearson Education.
3. Rao, N. N. (2021). Engineering Electromagnetics (8th ed.). Pearson Education.
4. Jordan, E. C., & Balmain, K. G. (2020). Electromagnetic Waves and Radiating Systems (2nd ed.). Pearson Education.
5. Bakshi, U. A., & Bakshi, A. V. (2023). Electromagnetic Field Theory (Revised ed.). Technical Publications.

2. Reference Books

1. Balanis, C. A. (2022). Advanced Engineering Electromagnetics (2nd ed.). Wiley.
2. Kraus, J. D., & Fleisch, D. A. (2020). Electromagnetics with Applications (6th ed.). McGraw Hill.
3. Paul, C. R. (2021). Fundamentals of Electromagnetic Fields (2nd ed.). Wiley.
4. Guru, B. S., & Hiziroglu, H. R. (2019). Electromagnetic Field Theory Fundamentals (3rd ed.). Cambridge University Press.
5. Murthy, T. V. S. A. (2022). Principles of Electromagnetic Field Theory (1st ed.). Cengage Learning.

3. E-Resources

1. NPTEL: Electromagnetic Fields.
   `https://nptel.ac.in/courses/108104087`
2. NPTEL: Transmission Lines and Electromagnetic Waves.
   `https://nptel.ac.in/courses/108106159`
3. MIT OpenCourseWare: Electromagnetics and Applications.
   `https://ocw.mit.edu/courses/electrical-engineering-and-computer-sci-ence-/6-007-electromagnetics-and-applications-spring-2011/`
4. All About Circuits: Electromagnetism Theory.
   `https://www.allaboutcircuits.com/textbook/electromagnetism/`
5. IEEE Xplore: Fundamentals of Electromagnetics for Engineers.
   `https://ieeexplore.ieee.org/`

Industrial Relevance

This course bridges the gap between theoretical physics and semiconductor engineering by providing the essential mathematical framework for signal integrity, power integrity, and interconnect design in VLSI systems. Understanding electromagnetic field behavior is critical for engineers developing high-speed integrated circuits where parasitic effects, electromagnetic interference (EMI), and transmission line discontinuities dictate the reliability and performance of modern silicon-based architectures.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	-	-	-	-	-	-	-	1	3	1	1
CO2	3	3	2	1	3	2	1	-	-	-	-	3	2	1
CO3	3	2	2	1	2	3	1	-	-	-	-	2	3	1
CO4	3	3	2	2	3	2	2	-	-	-	-	3	2	2
CO5	3	2	3	3	1	3	3	-	-	-	2	3	3	2
Weighted Average	3.00	2.40	2.00	1.75	2.25	2.50	1.75	-	-	-	1.00	2.80	2.20	1.40

Course Code: U23EVT04
Course Title: SystemVerilog
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design
SDG: 4,9

Course Overview

This course introduces SystemVerilog as a unified hardware description and verification language used in modern FPGA, ASIC, and SoC design environments. Building upon the digital design and verification fundamentals, students learn advanced language constructs, reusable RTL design methodologies, interface-based communication, assertion-based verification, functional coverage, and introductory object-oriented verification concepts. The course provides a strong foundation for advanced studies in SoC Design, RTL Verification, ASIC Design Flow, and Semiconductor Product Engineering.

Course Objectives

1. Explain advanced SystemVerilog language features used for digital design and verification.
2. Develop synthesizable and reusable RTL models using SystemVerilog constructs and methodologies.
3. Apply interface-based design techniques for modular and scalable hardware development.

Unit I: Introduction to System Verilog and Data Types **9 Hours**
System Verilog Overview-Motivation and Benefits over Verilog-Design and Verification Domains-Modules and Hierarchical Modeling Concepts-Extended Data Types: logic, bit, reg, byte, shortint, int, longint-2-State and 4-State Data Types-Enumerated Types-User Defined Types-Constants and Type Casting-Packed and Unpacked Arrays-Structures and Unions-Packages and Namespaces.
Active Learning Activity: Develop SystemVerilog models using advanced data types and compare their behavior with equivalent Verilog implementations.

Unit II: Procedural Statements and Control Flow Enhancements **9 Hours**
Procedural Blocks: initial, always, always_comb, always_ff-Blocking and Non-Blocking Assignments-Conditional Statements: if, if-else, case, casez, casex-Loop Constructs: for, foreach, while, do-while, repeat-Tasks and Functions-Return Types and Default Arguments-Void Functions-Time Control and Delay Mechanisms-Event Control and Triggering Mechanisms-Disabling Tasks and Control Constructs-Coding Guidelines for Synthesizable RTL.
Active Learning Activity: Model combinational and sequential circuits using advanced procedural constructs and analyze simulation behavior.

Unit III: Interfaces, Modports and Clocking Blocks **9 Hours**
Introduction to Interfaces-Purpose and Advantages of Interfaces-Interface Declaration and Instantiation-Interface-Based Communication-Modports and Access Restrictions-Reusability through Interfaces-Parameterized Interfaces-Clocking Block Syntax and Semantics-Default Clocking-Synchronous and Asynchronous Reset Concepts-Timing Isolation using Clocking Blocks-Interface-Based Design Methodology.
Active Learning Activity: Develop a modular digital design using interfaces and modports and

demonstrate communication between multiple RTL modules.

Unit IV: Assertions and Functional Coverage **9 Hours**
Verification-Immediate Assertions-Concurrent Assertions-Assertion Statements: assert, assume, and cover-Sequences and Property Definitions-Temporal Operators-Simple System Verilog Assertion (SVA) Examples-Assertion Debugging Techniques-Introduction to Functional Coverage-Covergroups and Coverpoints-Coverage Bins and Cross Coverage-Coverage Collection and Sampling Concepts-Verification Metrics Awareness.
Active Learning Activity: Create assertion-based checks for a digital design and measure functional coverage using covergroups and coverpoints.

Unit V: Advanced SystemVerilog Verification Concepts **9 Hours**
Overview of Object-Oriented Programming Concepts-Classes and Objects-Encapsulation-Inheritance-Polymorphism-Constructors-Random Variables and Constrained Randomization-Constraint Solving Concepts-Verification Component Concepts-Generator, Driver, Monitor, and Scoreboard Architecture-Transaction-Based Verification Fundamentals-Introduction to Universal Verification Methodology (UVM)-Class-Based Testbench Development.
Active Learning Activity: Develop a simple class-based verification environment incorporating random stimulus generation, monitoring, and result checking.

Course Outcomes (COs)

1. Explain SystemVerilog language features, advanced data types and modeling constructs used in digital design and verification. (K3)
2. Develop SystemVerilog-based hardware modules using procedural blocks and control flow constructs. (K3)
3. Construct reusable RTL designs using interfaces, modports and clocking blocks. (K3)
4. Analyze digital designs using assertions and functional coverage techniques. (K4)
5. Develop class-based verification environments using object-oriented SystemVerilog concepts and constrained-random methodologies. (K4)

Resources

1. Text Books

1. Sutherland, S., Davidmann, S., & Flake, P. (2019). SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling (2nd ed.). Springer.
2. Spear, C., & Tumbush, G. (2020). SystemVerilog for Verification (4th ed.). Springer.
3. Palnitkar, S. (2020). SystemVerilog for Verification: A Guide to Learning the Testbench Language Features (4th ed.). Pearson Education.
4. Perry, D. L., & Foster, H. (2021). Applied Digital Design and Verification Using SystemVerilog (2nd ed.). Wiley-IEEE Press.
5. Cohen, B., & Venkataramanan, S. (2022). SystemVerilog Assertions Handbook (4th ed.). VhdlCohen Publishing.

2. Reference Books

1. Bergeron, J. (2021). Writing Testbenches Using SystemVerilog (3rd ed.). Springer.
2. Mehta, A. B. (2021). Introduction to SystemVerilog: Concepts and Code. Springer.
3. Taraate, V. (2022). SystemVerilog for Hardware Description and Verification (2nd ed.). Springer.
4. Dubey, R. (2020). Introduction to Embedded System Design Using SystemVerilog. Springer.
5. Churiwala, S. (2019). Design Verification with e and SystemVerilog: A Comparative Guide. Springer.

3. E-Resources

1. NPTEL: System Design with Advanced Digital Design using Verilog/System Verilog
   `https://nptel.ac.in`
2. EDA Playground Online System Verilog Simulation Platform
   `https://www.edaplayground.com`
3. NPTEL: Digital Systems Design with PLDs and FPGAs
   `https://nptel.ac.in`
4. Verification Academy: System Verilog and Verification Methodologies
   `https://verificationacademy.com`
5. ASIC World: System Verilog Tutorials and Examples
   `http://www.asic-world.com`

Industrial Relevance

This course bridges the gap between digital hardware design and modern ASIC/SoC development practices. Students gain proficiency in SystemVerilog-based RTL modeling, reusable design methodologies, interface-based communication, assertion-based verification, functional coverage, and introductory object-oriented verification techniques. The course serves as a foundation for advanced studies in SoC Design, RTL Design and Verification, ASIC Front-End Design, FPGA Design, Functional Verification, and Semiconductor Product Engineering.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	1	1	1	1	-	-	-	1	-	2	1	1	1
CO2	3	2	2	2	2	-	-	-	1	-	1	3	2	2
CO3	3	2	3	2	2	-	-	1	1	-	2	3	3	2
CO4	3	3	2	3	3	1	-	1	1	-	2	3	3	2
CO5	3	3	3	3	3	1	1	2	2	1	3	3	3	3
Weighted Average	2.80	2.20	2.20	2.20	2.20	1.00	1.00	1.00	1.20	1.00	2.00	2.60	2.40	2.00

Course Code: U23EVT05
Course Title: Analog Integrated Circuits Design
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
Prerequisite(s): Electronic Devices and Circuits, Electric Circuits and Electron Devices
SDG: 7,9

Course Overview

This course provides a comprehensive exploration of the fundamental design principles and architectures of analog integrated circuits within modern silicon systems. It covers the transition from individual active components to complex, performance-optimized building blocks essential for data conversion and power management. Students will gain the engineering proficiency required to integrate these analog sub-systems into larger, sophisticated System-on-Chip environments.

Course Objectives

1. Analyze the design considerations and performance parameters for integrating analog functions in modern semiconductor processes.
2. Formulate high-performance analog building blocks, including current sources, differential amplifiers, and operational amplifiers, for diverse system requirements.
3. Evaluate signal conditioning, data conversion, power management, and clocking architectures to ensure system-level reliability and efficiency in mixed-signal applications.

Unit I: Introduction to Analog Integrated Circuits **9 Hours**
Evolution of Integrated Circuits-Analog and Digital Integrated Circuits-Characteristics of Analog Signals-Analog IC Design Considerations-Performance Parameters: Gain, Bandwidth, Noise, Offset and Power Dissipation-Process Variations-Device Matching Concepts-Analog Building Blocks in Integrated Circuits-Overview of Analog and Mixed-Signal Systems.
Active Learning Activity: Conduct a comparative study identifying analog functional blocks present in mobile devices and explain their circuit purpose.
Unit II: Fundamental Analog Building Blocks **9 Hours**
Current Sources-Current Mirrors-Differential Amplifier Concepts-Operational Amplifier Fundamentals-Comparator Fundamentals-Schmitt Trigger-Voltage Follower-Analog Signal Amplification Concepts-Performance Parameters of Analog Building Blocks.
Active Learning Activity: Perform a simulation-based design of a differential amplifier to analyze gain and bandwidth using open-source circuit simulation tools.
Unit III: Signal Conditioning and Data Conversion **9 Hours**
Signal Conditioning Concepts-Sensor Interface Fundamentals-Instrumentation Concepts-Sample-and-Hold Circuits-Analog-to-Digital Conversion- Fundamentals-Digital-to-Analog Conversion Fundamentals-Resolution-Accuracy-Quantization Concepts-Applications of Data Converters in Mixed-Signal Systems.
Active Learning Activity: Compare the performance metrics of ADCs and DACs through a laboratory-based evaluation of conversion speed and accuracy.
Unit IV: Power Management and Timing Circuits **9 Hours**
Voltage Reference Concepts-Bandgap Reference Overview-Voltage Regulation Fundamentals-Low Dropout Regulator Overview-Power Management IC Concepts-Oscillator Fundamentals-

Ring Oscillator Concept-Phase-Locked Loop Overview-Clock Generation in Integrated Systems.
Active Learning Activity: Analyze the power management and clock generation architecture of a portable electronic device through a structural block diagram study.

Unit V: Analog IC Applications in Modern Systems **9 Hours**

Analog Front-End Concepts-Mixed-Signal System Integration-Power Management IC Applications-Analog Interfaces in Communication Systems-Automotive Electronics Applications-Biomedical Electronics Applications-IoT Sensor Interfaces-Future Trends in Analog-Mixed-Signal IC Design.
Active Learning Activity: Present a technical case study on the application of specific analog integrated circuits in a modern semiconductor hardware product.

Course Outcomes (COs)

CO1: Explain the fundamentals and performance characteristics of analog integrated circuits used in electronic systems. (K3)
CO2: Describe the operation of fundamental analog building blocks used in integrated circuits. (K3)
CO3: Apply signal conditioning and data conversion concepts in mixed-signal electronic systems. (K3)
CO4: Analyze power management and timing circuits employed in integrated systems. (K4)
CO5: Evaluate the role of analog integrated circuits in modern embedded and system-on-chip-based applications. (K4)

Resources

1. Text Books

1. Razavi, B. (2021). Design of Analog CMOS Integrated Circuits (2nd ed.). McGraw-Hill Education.
2. Baker, R. J. (2019). CMOS: Circuit Design, Layout and Simulation (4th ed.). Wiley-IEEE Press.
3. Gray, P. R., Hurst, P. J., Lewis, S. H., & Meyer, R. G. (2022). Analysis and Design of Analog Integrated Circuits (6th ed.). Wiley.
4. Johns, D. A., & Martin, K. (2023). Analog Integrated Circuit Design (2nd ed.). Wiley.
5. Sedra, A. S., & Smith, K. C. (2020). Microelectronic Circuits (8th ed.). Oxford University Press.

2. Reference Books

1. Sansen, W. M. C. (2023). Analog Design Essentials (2nd ed.). Springer.
2. Allen, P. E., & Holberg, D. (2022). CMOS Analog Circuit Design (4th ed.). Oxford University Press.
3. Franco, S. (2016). Design with Operational Amplifiers and Analog Integrated Circuits (4th ed.). McGraw-Hill Education.
4. Razavi, B. (2021). Fundamentals of Microelectronics (3rd ed.). Wiley.
5. Carusone, T. C., Johns, D., & Martin, K. (2024). Analog Integrated Circuit Design (3rd ed.). Wiley.

3. E-Resources

1. NPTEL Analog Electronic Circuits
   `https://nptel.ac.in/courses/108106070`
2. NPTEL Analog CMOS VLSI Design
   `https://nptel.ac.in/courses/108106142`
3. MIT OpenCourseWare: Analog Integrated Circuit Design
   `https://ocw.mit.edu/`
4. Analog Devices Education Library
   `https://www.analog.com/en/education.html`
5. Texas Instruments Analog Engineer's Circuit Resources
   `https://www.ti.com/design-resources/`

Industrial Relevance

This course bridges the gap between theoretical semiconductor physics and practical chip-level implementation, which is the backbone of the global semiconductor industry. By mastering the design of building blocks like LDOs, PLLs, and data converters, students gain the expertise required for roles in system-on-chip design, analog front-end engineering, and power management IC development. This curriculum prepares students for the rapid scaling and mixed-signal integration challenges faced by modern giants in the automotive, IoT, and high-performance computing sectors.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	1	1	1	-	-	-	-	1	2	1	1
CO2	3	2	1	1	1	-	-	-	-	-	2	1	1	1
CO3	3	3	2	2	2	1	-	1	1	1	2	3	2	2
CO4	3	3	3	3	3	1	-	1	1	1	2	3	3	2
CO5	3	3	3	3	3	2	1	1	1	1	2	3	3	3
Weighted Average	3.00	2.60	2.00	2.00	2.00	1.20	1.00	1.00	1.00	1.00	1.80	2.40	2.00	1.80

Course Code: U23EVT06
Course Title: CMOS Integrated Circuits
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
Pre-Requisites: Digital System Design, Electronic Devices and Circuits
SDG: 7,9,12

Course Overview

This course provides a comprehensive understanding of CMOS technology, fabrication processes, and design principles for digital integrated circuits. It focuses on developing the ability to design and analyze combinational, sequential, and subsystem-level circuits with considerations for power, performance, and reliability. Additionally, the course equips learners with knowledge of low-power design techniques, testability methods, and modern CMOS design challenges to prepare them for advanced applications in VLSI design.

Course Objectives

1. To provide a comprehensive understanding of CMOS technology, fabrication processes, and design principles for digital integrated circuits.
2. To develop the ability to design and analyze combinational, sequential, and subsystem-level circuits with considerations for power, performance, and reliability.
3. To equip learners with knowledge of low-power design techniques, testability methods, and modern CMOS design challenges to prepare them for advanced applications in VLSI design.

Unit I: Introduction to CMOS Technology and Fabrication **9 Hours**
CMOS fabrication process-p-well technology-n-well technology-twin-tub technology-Layout design rules-lambda-based design rules-Stick diagrams-inverter layout using stick diagrams-Process enhancements for performance scaling and reliability.
Active Learning Activity: Students will create physical layout representations for a CMOS inverter using lambda-based design rules to bridge schematic-to-layout concepts.
Unit II: CMOS Inverter and Combinational Logic Gates **9 Hours**
Logical effort-transistor sizing strategies-performance optimization-complex CMOS combinational logic gates-XOR gate design-multiplexers-AOI/OAI gates-Transmission gate-based logic-Interconnect parasitics impact-Low-skew clock distribution.
Active Learning Activity: Students will perform an analytical study comparing the propagation delay and area requirements of AOI versus OAI complex gates.
Unit III: Sequential Circuits and Memory Elements **9 Hours**
Basic sequential circuit elements-Latch design-Flip-Flops using CMOS-Timing considerations-Setup time-Hold time-Dynamic storage elements-Pseudo-static registers-Schmitt trigger design-CMOS SRAM cell architecture.
Active Learning Activity: Students will simulate timing constraints for a D-flip-flop to determine the operational frequency limits under parasitic loading.
Unit IV: CMOS Subsystem Design and Arithmetic Circuits **9 Hours**
Ripple Carry Adder-Carry Look Ahead Adder-Subtractors-Array Multipliers-Booth Multipliers-Comparators-Barrel shifter-CMOS multiplexer and decoder-Control logic and bus structures.
Active Learning Activity: Students will design and evaluate the modular layout of a 4-bit Ripple Carry Adder emphasizing regularity and signal routing efficiency.

Unit V: CMOS Design for Low Power and Testability **9 Hours**

Sources of power dissipation-Dynamic power analysis-Static power analysis-Clock gating techniques-Multi-Vdd design-Power gating methods-Scan-based test-Built-in Self-Test-Fault models and reliability.

Active Learning Activity: Students will construct a comparative report on the efficacy of clock gating versus power gating in reducing total power consumption.

Course Outcomes (COs)

CO1: Explain the CMOS fabrication process, layout design rules, and scaling methods to demonstrate understanding of integrated circuit technology. (K3)

CO2: Apply transistor sizing and logical effort principles to design and evaluate CMOS inverters and combinational logic circuits. (K3)

CO3: Analyze the operation of sequential circuits and memory elements, including latches, flip-flops, SRAM cells, and non-volatile memory basics. (K4)

CO4: Design arithmetic subsystems such as adders, multipliers, comparators, and bus structures, with emphasis on performance and layout optimization. (K3)

CO5: Evaluate power dissipation sources and testability issues in CMOS circuits, and apply low-power and DFT techniques to improve design efficiency. (K4)

Resources

1. Text Books

1. Abbas, K. (2020). Handbook of digital CMOS technology, circuits, and systems (1st ed.). Springer.
2. Baker, R. J. (2019). CMOS: Circuit design, layout, and simulation (4th ed.). Wiley-IEEE Press.
3. Razavi, B. (2020). Design of CMOS phase-locked loops (1st ed.). Cambridge University Press.
4. Veendrick, H. (2025). Nanometer CMOS ICs: From basics to ASICs (3rd ed.). Springer.
5. Yang, X. (2022). Integrated circuit design: IC design flow and project-based learning (1st ed.).

2. Reference Books

1. Weste, N. H. E., & Harris, D. (2019). CMOS VLSI design: A circuits and systems perspective (5th ed.). Pearson.
2. Zjajo, A. (2020). Low-power high-resolution analog-to-digital converters: Design and architectures (1st ed.). Springer.
3. Ray, A. K., & Ganguly, A. (2022). Low power VLSI design: Classical and emerging techniques (1st ed.). CRC Press.
4. Gray, P. R., Hurst, P. J., Lewis, S. H., & Meyer, R. G. (2023). Analysis and design of analog integrated circuits (6th ed.). Wiley.

5. Friedman, E. G. (Ed.). (2021). Power distribution networks in high speed integrated circuits (2nd ed.). Springer.

3. E-Resources

1. NPTEL: Digital VLSI Design (Note: Fundamentals and Logic Gates)
   `https://nptel.ac.in/courses/117/106/117106092`
2. NPTEL: CMOS Digital VLSI Design (Note: Fabrication and Sequencing)
   `https://nptel.ac.in/courses/106/105/106105186`
3. MOOC: VLSI CAD: Logic to Layout
   `https://www.coursera.org/learn/vlsi-cad-logic-to-layout`
4. IEEE Xplore: CMOS and VLSI Journals
   `https://ieeexplore.ieee.org`
5. Semiconductor Engineering: Insights on Low Power and Testability
   `https://semiengineering.com`

Industrial Relevance

This course bridges the gap between academic theory and industry practice by focusing on the physical implementation, power optimization, and design-for-testability standards critical to the modern semiconductor industry. By mastering CMOS fabrication, layout strategies, and low-power design methodologies, students gain the technical proficiency required to design complex integrated systems that meet the rigorous performance and reliability demands of global hardware companies.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	-	2	-	-	-	-	-	-	3	-	-
CO2	3	3	3	-	2	-	-	-	1	-	-	3	2	-
CO3	3	3	2	2	2	-	-	-	-	-	-	2	3	-
CO4	3	2	3	-	3	-	-	-	2	1	-	3	3	2
CO5	3	3	2	2	2	-	2	-	-	-	1	-	3	3
Weighted Average	3.00	2.60	2.20	2.00	2.20	-	2.00	-	1.50	1.00	1.00	2.75	2.75	2.50

Course Code: U23ECP10
Course Title: Linear Integrated Circuits Laboratory
Course Type: Professional Core Laboratory
L T P C: 0 0 4 2
Total Periods: 60

Course Overview

This laboratory course is designed to provide hands-on experience in the design, implementation, and analysis of fundamental linear integrated circuits. Students develop practical skills in circuit construction, simulation, performance measurement, and signal characterization using operational amplifiers and timers. The course is highly relevant to the electronics, communication, and VLSI industries, where precise analog signal processing and robust circuit design are critical.

Course Objectives

1. To gain hands-on experience in designing electronic circuits.
2. To learn simulation software used in circuit design.
3. To learn the fundamental principles of amplifier circuits, oscillators, and multivibrators.

Laboratory Experiments

Experiment 1: Inverting, Non inverting and differential amplifier (CO1)
Experiment 2: Integrator and Differentiator (CO1)
Experiment 3: Instrumentation Amplifier (CO2)
Experiment 4: Active filters (CO2)
Experiment 5: Astable & Monostable multivibrators using Op-amp (CO2)
Experiment 6: Schmitt Trigger using op-amp (CO2)
Experiment 7: Astable and Monostable multivibrators using NE555 Timer (CO2)
Experiment 8: Wien Bridge Oscillator using OP-AMP (CO2)
Experiment 9: RC Phase Shift Oscillator using OP-AMP (CO2)
Experiment 10: PLL Characteristics and its use as frequency multiplier, Clock Synchronization (CO3)

Course Outcomes

CO1: Analyze various types of feedback amplifiers. (K4)
CO2: Design oscillators, tuned amplifiers, wave-shaping circuits and multivibrators. (K3)
CO3: Design filters using op-amp and perform an experiment on frequency response. (K3)

Resources

Text Books

1. Roy D. Choudhry and Shail Jain, "Linear Integrated Circuits", 5th Edition, 2018, New Age International Pvt. Ltd., Edition.

2. Sergio Franco, "Design with Operational Amplifiers and Analog Integrated Circuits", 4th Edition, Tata McGraw-Hill, 2016.

Reference Books

1. Ramakant A. Gayakwad, "OP-AMP and Linear ICs", 4th Edition, Prentice Hall / Pearson Education, 2015.
2. Robert F. Coughlin, Frederick F. Driscoll, "Operational Amplifiers and Linear Integrated Circuits", 6th Edition, PHI, 2001.
3. Salivahanan S. Kanchana Bhaskaran V.S., "Linear Integrated Circuits", TMH, 2nd Edition, 4th Reprint, 2016.

E-Resources

`https://nptel.ac.in/courses/108108111`
`https://nptel.ac.in/courses/117107094`
`https://onlinecourses.nptel.ac.in/noc24ee73/preview`
`https://nptel.ac.in/courses/108105157`
`https://nptel.ac.in/courses/108107142`

Industrial Relevance

This laboratory develops core competencies in measurement, instrumentation, and hardware implementation, which are essential for engineers working in the semiconductor and embedded systems sectors. By engaging in circuit debugging, validation, and performance verification, students acquire the technical discipline required to troubleshoot complex analog systems. These skills directly translate into the industry's need for proficient personnel capable of designing, testing, and optimizing integrated circuits for diverse communication and VLSI applications.

CO–PO–PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	-	2	-	-	-	-	3	3	3	2
CO2	-	-	-	-	-	-	-	-	-	-	-	2	1	2
CO3	-	3	3	2	-	2	-	-	-	-	2	2	3	2
Weighted Average	3.00	2.50	2.50	2.00	0.00	2.00	0.00	0.00	0.00	0.00	2.50	2.33	2.33	2.00

Course Code: U23EVP03
Course Title: Hardware modelling Using SystemVerilog Laboratory
Course Type: Professional Core Laboratory
L T P C: 0 0 4 2
Total Hours: 60
SDG: 4,9

Course Overview

This laboratory course aims to provide comprehensive practical experience in designing, modeling, and verifying complex digital systems using advanced SystemVerilog hardware description and verification constructs. Students develop critical practical skills in modular hardware architecture, clock timing isolation, assertion-based error detection, functional coverage analysis, and object-oriented testbench implementation using open-source academic EDA simulation tools. The competencies acquired are directly relevant to the semiconductor, communications, and VLSI industries, preparing students for industry-standard ASIC and FPGA verification engineering workflows.

Course Objectives

1. To design and simulate synthesizable combinational and sequential digital circuits using advanced SystemVerilog data types, procedural constructs, interfaces, and modports.
2. To implement robust timing isolation and verification environments utilizing clocking blocks, SystemVerilog assertions, and functional coverage models.
3. To develop scalable, object-oriented, and constrained-random verification testbenches to systematically validate complex digital hardware modules against functional specifications.

Laboratory Experiments

Experiment 1: Implementation of Advanced Data Types (CO1)
Develop and simulate a digital design using advanced SystemVerilog data types and compare the results with equivalent Verilog models.

Experiment 2: Design Using Enumerated and User Defined Types (CO1)
Design a digital module using enumerated and user-defined data types, simulate its functionality, and present the results.

Experiment 3: Procedural Modeling of Combinational Circuits (CO2)
Design and verify a combinational digital circuit using procedural constructs and analyze the simulation results.

Experiment 4: Sequential Circuit Design and Time Control (CO2)
Design and simulate a sequential digital circuit using appropriate timing control and verify its functional behavior.

Experiment 5: Modular Design Using Interfaces and Modports (CO3)
Develop a modular digital design using interfaces and modports, verify its functionality, and present the simulation results.

Experiment 6: Clocking Blocks and Timing Isolation (CO3)
Implement clocking blocks in a verification environment, simulate the design, and analyze timing behavior.

Experiment 7: Assertion-Based Verification (CO4)
Design and verify a digital module using SystemVerilog assertions to detect functional errors during simulation.

Experiment 8: Functional Coverage Analysis (CO4)
Develop functional coverage models for a digital design, analyze the coverage results, and identify uncovered scenarios.

Experiment 9: Object-Oriented Verification Environment (CO5)
Develop a class-based verification environment, verify the functionality of a digital design, and present the verification results.

Experiment 10: Constrained-Random Verification (CO5)
Design and verify a digital hardware module using constrained-random verification techniques, analyze the simulation results, and present the verification report.

Course Outcomes

Upon completion of this laboratory course, the students will be able to:

- **CO1:** Model digital circuits using advanced SystemVerilog data types, enumerated types, and user-defined constructs. (K3)
- **CO2:** Design and verify combinational and sequential digital circuits using advanced procedural constructs and timing controls. (K4)
- **CO3:** Implement modular hardware designs and isolated timing environments utilizing interfaces, modports, and clocking blocks. (K3)
- **CO4:** Apply assertion-based verification and functional coverage models to detect logic errors and analyze verification completeness. (K4)
- **CO5:** Develop object-oriented and constrained-random verification environments for comprehensive digital design verification. (K5)

Resources

Text Books

1. Spear, C., & Tumba, G. (2012). *SystemVerilog for verification: A guide to learning the testbench language features* (3rd ed.). Springer.
2. Sutherland, S., Davidmann, S., & Flake, P. (2006). *SystemVerilog for design: A guide to using SystemVerilog for hardware design and modeling* (2nd ed.). Springer.

Reference Books

1. Salimi, S. (2019). *Comprehensive SystemVerilog: For design and verification.* IEEE Press.
2. Vijayaraghavan, S., & Ramanathan, M. (2005). *A practical guide for SystemVerilog assertions.* Springer.

3. Bergeron, J. (2012). *Writing testbenches using SystemVerilog* (2nd ed.). Springer.

E-Resources

1. `https://www.asic-world.com/systemverilog/tutorial.html`
2. `https://www.verificationacademy.com/topics/systemverilog`
3. `https://www.doulos.com/knowhow/systemverilog/`
4. `https://www.chipverify.com/systemverilog/systemverilog-tutorial`
5. `https://www.edaplayground.com/`

Industrial Relevance

This laboratory course develops essential practical competencies by translating advanced hardware modeling theory into rigorous verification practice. Through structured experimentation with open-source simulation environments, students cultivate precise measurement skills and instrumentation skills by analyzing digital waveforms, timing relationships, propagation delays, and clock domain anomalies. The curriculum enhances hardware implementation skills and circuit debugging capabilities by requiring students to systematically isolate logic faults, resolve timing violations, and construct modular interconnects using interfaces and clocking blocks. Furthermore, the implementation of assertion-based verification, functional coverage analysis, and constrained-random test generation equips students with industry-standard validation and verification techniques necessary for rigorous communication system testing and functional sign-off. These comprehensive design and verification proficiencies are of immense relevance to the semiconductor, communication, embedded systems, and VLSI industries, directly enabling graduates to architect and verify first-pass silicon designs for complex Application-Specific Integrated Circuits (ASICs) and Field-Programmable Gate Arrays (FPGAs).

CO–PO–PSO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	2	2	2	3	3	–	–	2	2	–	2	3	3	2
CO2	3	3	3	3	3	–	–	2	2	–	2	3	3	2
CO3	2	2	3	3	3	–	–	3	2	–	2	3	3	2
CO4	3	3	3	3	3	–	1	3	3	–	3	3	3	3
CO5	3	3	3	3	3	–	1	3	3	1	3	3	3	3
Weighted Average	**2.60**	**2.60**	**2.80**	**3.00**	**3.00**	**–**	**1.00**	**2.60**	**2.40**	**1.00**	**2.40**	**3.00**	**3.00**	**2.40**

Course Code: U23EVP04
Course Title: CMOS IC laboratory
Course Type: Professional Core Laboratory
L T P C: 0 0 4 2
Total Hours: 60
SDG: 7,9,12

Course Overview

This laboratory course provides a comprehensive practical foundation in CMOS technology, physical design, and integrated circuit implementation. Students develop technical proficiency in designing, simulating, and verifying digital circuits, memory elements, and arithmetic subsystems. These skills are essential for addressing the performance, reliability, and power-efficiency requirements of the modern semiconductor, communication, and VLSI industries.

Course Objectives

1. To provide hands-on experience in CMOS layout design and fabrication-related design rules.
2. To develop skills in designing and verifying combinational, sequential, and arithmetic circuits using industry-standard design flows.
3. To equip learners with methods to evaluate power dissipation and testability in digital integrated circuits.

Laboratory Experiments

Experiment 1: CMOS Fabrication and Layout Design Rules (CO1)
Design and layout of a basic CMOS inverter using lambda-based design rules to visualize physical layers.
Experiment 2: Stick Diagram Implementation (CO1)
Implementation of CMOS inverter stick diagrams to understand the mapping between schematic and physical layout.
Experiment 3: Logical Effort and Transistor Sizing (CO2)
Analysis of propagation delay and performance optimization through transistor sizing strategies for CMOS inverters.
Experiment 4: Complex Combinational Logic Gate Design (CO2)
Design and performance comparison of complex AOI/OAI gates and multiplexer architectures.
Experiment 5: Sequential Circuit Element Analysis (CO3)
Design and characterization of CMOS latches and flip-flops to observe clocking and state retention.
Experiment 6: Timing Constraint Verification (CO3)
Measurement of setup and hold time constraints for D-flip-flops under various loading conditions.
Experiment 7: Arithmetic Subsystem Design (CO4)
Implementation of Ripple Carry Adders and Carry Look Ahead Adders to evaluate architectural efficiency.
Experiment 8: Multipliers and Data Path Components (CO4)
Design and simulation of array multipliers and barrel shifters for high-performance arithmetic applications.

Experiment 9: Power Dissipation Analysis (CO5) Measurement and analysis of static and dynamic power consumption in CMOS digital circuits.
Experiment 10: Fault Modeling and Testability Assessment (CO5)
Implementation of scan-based test structures and evaluation of fault models to ensure circuit reliability.

Course Outcomes

CO1: Explain the CMOS fabrication process, layout design rules, and scaling methods to demonstrate understanding of integrated circuit technology. (K3)
CO2: Apply transistor sizing and logical effort principles to design and evaluate CMOS inverters and combinational logic circuits. (K3)
CO3: Analyze the operation of sequential circuits and memory elements, including latches, flip-flops, SRAM cells, and non-volatile memory basics. (K4)
CO4: Design arithmetic subsystems such as adders, multipliers, comparators, and bus structures, with emphasis on performance and layout optimization. (K3)
CO5: Evaluate power dissipation sources and testability issues in CMOS circuits, and apply low-power and DFT techniques to improve design efficiency. (K4)

Resources

Text Books

1. Abbas, K. (2020). Handbook of digital CMOS technology, circuits, and systems (1st ed.). Springer.
2. Baker, R. J. (2019). CMOS: Circuit design, layout, and simulation (4th ed.). Wiley-IEEE Press.
3. Razavi, B. (2020). Design of CMOS phase-locked loops (1st ed.). Cambridge University Press.
4. Veendrick, H. (2025). Nanometer CMOS ICs: From basics to ASICs (3rd ed.). Springer.
5. Yang, X. (2022). Integrated circuit design: IC design flow and project-based learning (1st ed.).

Reference Books

1. Weste, N. H. E., & Harris, D. (2019). CMOS VLSI design: A circuits and systems perspective (5th ed.). Pearson.
2. Zjajo. A. (2020). Low-power high-resolution analog-to-digital converters: Design and architectures (1st ed.). Springer.
3. Ray, A. K., & Ganguly, A. (2022). Low power VLSI design: Classical and emerging techniques (1st ed.). CRC Press.
4. Gray, P. R., Hurst, P. J., Lewis, S. H., & Meyer, R. G. (2023). Analysis and design of analog integrated circuits (6th ed.). Wiley.
5. Friedman, E. G. (Ed.). (2021). Power distribution networks in high speed integrated circuits (2nd ed.). Springer.

E-Resources

1. `https://nptel.ac.in/courses/117/106/117106092`
2. `https://nptel.ac.in/courses/106/105/106105186`
3. `https://www.coursera.org/learn/vlsi-cad-logic-to-layout`

4. `https://ieeexplore.ieee.org`
5. `https://semiengineering.com`

Industrial Relevance

This laboratory course is vital for bridging the gap between theoretical knowledge and industry requirements by focusing on practical measurement and instrumentation skills. Students gain hands-on experience in hardware implementation, circuit debugging, and validation techniques, which are critical for the design, testing, and verification phases in the semiconductor and VLSI industries. Through systematic investigation of power and timing constraints, learners become proficient in using industry-standard workflows that ensure the reliability and efficiency of integrated systems in embedded and communication applications.

CO–PO–PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	2	2	-	-	1	1	-	-	3	2	-
CO2	3	3	3	3	3	-	-	2	2	-	-	3	2	-
CO3	3	3	2	3	3	-	-	2	2	-	-	2	3	-
CO4	3	2	3	3	3	-	-	2	2	-	-	3	3	2
CO5	3	3	2	3	3	-	-	2	2	-	1	2	3	3
Weighted Average	3.00	2.60	2.20	2.80	2.80	-	-	1.80	1.80	-	1.00	2.60	2.60	2.50

Course Code: U23EVT07
Course Title: Digital Signal Processing Algorithms
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design, Probability and Random Processes
SDG: 9

Course Overview

This course provides a foundational exploration of discrete-time signal processing, bridging the gap between mathematical transform techniques and practical hardware realization. Students will analyze signals and systems in both time and frequency domains while evaluating the computational efficiency of algorithms like DFT and FFT. The curriculum culminates in the design of digital filters and the architectural optimization of DSP systems for FPGA and ASIC platforms.

Course Objectives

1. Develop proficiency in representing and analyzing discrete-time signals and systems through time-domain operations and difference equations.
2. Master frequency-domain analysis tools, specifically the Z-transform, DFT, and FFT, to solve complex spectral computation problems.
3. Evaluate hardware architectures for FIR and IIR filters, focusing on trade-offs in speed, area, and power consumption for VLSI implementation.

Unit I: Discrete-Time Signals and Systems **9 Hours**
Introduction to Digital Signal Processing applications – Continuous-time and discrete-time signals – Basic discrete-time signals and signal operations – Discrete-time systems and properties (linearity, causality, time invariance and stability) – Convolution of discrete-time signals – Difference equation representation of systems – Applications of DSP in communication and multimedia systems.
Active Learning Activity: Visualization of discrete-time signals and convolution using computational tools.
Unit II: Transform Techniques for DSP **9 Hours**
Frequency-domain representation of signals – Discrete-Time Fourier Transform (DTFT) – Properties of DTFT – Sampling theorem and aliasing – Introduction to Z-Transform – Region of Convergence (ROC) – Basic properties of Z-Transform – Signal and system analysis using transform techniques.
Active Learning Activity: Spectrum analysis of sampled signals using simulation tools.
Unit III: DFT and FFT Algorithms **9 Hours**
Discrete Fourier Transform (DFT) – Properties of DFT – Circular and linear convolution using DFT – Need for Fast Fourier Transform (FFT) – Radix-2 Decimation-in-Time FFT – Radix-2 Decimation-in-Frequency FFT – Butterfly structures – Computational complexity comparison of DFT and FFT.
Active Learning Activity: Simulation and comparison of DFT and FFT implementations.
Unit IV: Digital Filter Design **9 Hours**
Introduction to digital filters – FIR and IIR filter characteristics – Comparison of FIR and IIR filters – FIR filter design using Hamming Window method – Introduction to IIR filters and basic realization concepts – Direct-form and cascade realizations – Fixed-point realization issues and

quantization effects in digital filters.
Active Learning Activity: Design and analysis of FIR and IIR filters using computational tools.

Unit V: DSP Architectures and Hardware Realization **9 Hours**

Introduction to DSP processor architecture – Multiply-Accumulate (MAC) operation – Fixed-point arithmetic for DSP systems – FIR filter hardware architectures and transposed FIR structure – Pipelining concepts in DSP hardware – Memory considerations in DSP systems – Overview of FPGA and ASIC realization of DSP blocks – Area, speed and power trade-offs.
Active Learning Activity: Evaluation of DSP hardware architectures and implementation trade-offs through simulation.

Course Outcomes

CO1: Explain the fundamental concepts of discrete-time signals and systems used in DSP applications. (K2)
CO2: Apply transform techniques for frequency-domain analysis of signals and systems. (K3)
CO3: Analyze DFT and FFT algorithms for efficient spectral processing applications. (K4)
CO4: Analyze FIR and IIR digital filters and evaluate their characteristics. (K4)
CO5: Evaluate DSP hardware architectures and implementation trade-offs for FPGA and ASIC realization. (K5)

Resources

1. Text Books

1. Proakis, J. G., & Manolakis, D. G. (2023). Digital Signal Processing: Principles, Algorithms, and Applications (5th ed.). Pearson.
2. Oppenheim, A. V., & Schafer, R. W. (2021). Discrete-Time Signal Processing (4th ed.). Pearson.
3. Ifeachor, E. C., & Jervis, B. W. (2020). Digital Signal Processing: A Practical Approach (3rd ed.). Pearson.
4. Mitra, S. K. (2022). Digital Signal Processing: A Computer-Based Approach (5th ed.). McGraw-Hill Education.
5. Smith, S. W. (2019). The Scientist and Engineer's Guide to Digital Signal Processing (2nd ed.). California Technical Publishing.

2. Reference Books

1. Chen, C. T. (2020). Digital Signal Processing: Spectral Computation and Filter Design. Oxford University Press.
2. Lueder, E. (2021). Digital Filters and Signal Processing (3rd ed.). Springer.
3. Parhi, K. K. (2022). VLSI Digital Signal Processing Systems: Design and Implementation. Wiley.
4. Lyons, R. G. (2023). Understanding Digital Signal Processing (4th ed.). Addison-Wesley.
5. Hayes, M. H. (2020). Schaum's Outline of Digital Signal Processing (2nd ed.). McGraw-Hill.

3. E-Resources

1. IEEE Signal Processing Society Resource Center
`https://signalprocessingsociety.org/`
2. MIT OpenCourseWare: Digital Signal Processing
`https://ocw.mit.edu/courses/res-6-008-digital-signal-processing-spring-2011/`
3. DSP Related - Community and Tutorials

https://www.dsprelated.com/
4. Xilinx DSP Solution Center
https://www.xilinx.com/products/design-tools/dsp-solution-center.html
5. MathWorks DSP System Toolbox Documentation
https://www.mathworks.com/help/dsp/index.html

Industrial Relevance

This course serves as a critical bridge between theoretical signal processing and the high-performance requirements of modern silicon design. By shifting focus from pure mathematical abstraction to architectural implementation, students gain insights into the hardware-level challenges of MAC unit efficiency, fixed-point quantization, and pipelining—key parameters for ASIC/FPGA deployment in 5G communications, AI-driven edge computing, and real-time multimedia processors.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	1	1	-	-	-	-	-	1	2	1	1
CO2	3	3	2	2	2	-	-	-	-	-	1	2	1	1
CO3	3	3	2	3	3	-	-	-	-	-	2	3	2	1
CO4	3	3	3	3	3	1	-	-	-	-	2	3	2	2
CO5	3	3	3	3	3	1	-	1	1	1	2	3	3	2
Weighted Average	3.00	2.80	2.20	2.40	2.40	1.00	-	1.00	1.00	1.00	1.60	2.60	1.80	1.40

Course Code: U23EVT08
Course Title: Computer Architecture and On-Chip Communication
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design
SDG: 9

Course Overview

This course provides a comprehensive exploration of modern computer architecture and the intricate on-chip communication mechanisms essential for contemporary System-on-Chip design. Students engage with fundamental processor organization, instruction execution pipelines, memory hierarchy, and advanced interconnect frameworks. The curriculum emphasizes the architectural foundations required to analyze and model complex, high-performance semiconductor systems.

Course Objectives

1. To understand the functional organization, operation, and instruction cycle management of modern computer architectures.
2. To analyze performance optimization techniques including pipelining, memory hierarchy, and input/output system efficiency.
3. To examine on-chip communication paradigms, multicore architectures, and specialized network-on-chip frameworks in complex SoC platforms.

Unit I: Fundamentals of Computer Organization **9 Hours**
Computer system functional units-Von Neumann architecture-CPU organization-Memory organization-Input/Output organization-Register organization-Instruction cycle operations-Arithmetic Logic Unit operations-Data representation-Performance metrics.
Active Learning Activity: Trace the execution of a simple instruction through the functional units of a computer system.
Unit II: Processor Architecture and Pipelining **9 Hours**
Instruction formats-Addressing modes-Processor datapath organization-Control unit concepts-Instruction execution process-Basic Instruction Set Architecture-Pipelining concepts-Pipeline stages-Hazard detection and handling techniques.
Active Learning Activity: Analyze instruction execution in a pipelined processor and identify hazard conditions.
Unit III: Memory and Input/Output Organization **9 Hours**
Memory hierarchy-Locality of reference-Cache memory fundamentals-Cache mapping techniques-Cache hit and miss concepts-Main memory organization-Virtual memory concepts-Address translation basics-Input/Output performance considerations.
Active Learning Activity: Compare different levels of memory hierarchy and evaluate their impact on system performance.
Unit IV: On-Chip Communication and Bus Architectures **9 Hours**
Need for on-chip communication-Processor-memory-peripheral interconnects-Shared bus architecture-Synchronous and asynchronous buses-Bus arbitration techniques-Bus bandwidth and latency-Standard bus architecture concepts-System interconnect communication.
Active Learning Activity: Study data transfer between processor, memory, and peripherals using different bus architectures.

Unit V: Multicore Systems and Network-on-Chip **9 Hours**

Multicore processor introduction-Multicore architecture challenges-Shared memory concepts-Parallel processing basics-Network-on-Chip fundamentals-Network-on-Chip components-Mesh topology and routing concepts-Network performance considerations-Heterogeneous multicore and accelerator systems.

Active Learning Activity: Analyze the communication structure of a multicore system and identify the role of on-chip networks in data transfer.

Course Outcomes (COs)

CO1: Explain the organization and operation of computer systems and processor components. (K2)
CO2: Apply processor architecture and pipelining concepts to improve instruction execution performance. (K3)
CO3: Analyze memory hierarchy and input/output organization for efficient system operation. (K4)
CO4: Explain on-chip communication mechanisms and standard-based interconnect architectures used in SoC platforms. (K2)
CO5: Analyze multicore architectures and network-on-chip communication mechanisms in modern SoC platforms. (K4)

Resources

1. Text Books

1. Patterson, D. A., & Hennessy, J. L. (2021). *Computer organization and design RISC-V edition: The hardware software interface* (2nd ed.). Morgan Kaufmann.
2. Stallings, W. (2022). *Computer organization and architecture: Designing for performance* (11th ed.). Pearson.
3. Jha, N. K., & Jha, S. (2020). *Network-on-chip: The next generation of system-on-chip integration*. Springer.
4. Hamacher, C., Vranesic, Z., Zaky, S., & Manjikian, N. (2021). *Computer organization and embedded systems* (6th ed.). McGraw-Hill.
5. Wolf, M. (2020). *Modern VLSI design: System-on-chip design* (5th ed.). Pearson.

2. Reference Books

1. Dally, W. J., & Towles, B. P. (2022). *Principles and practices of interconnection networks*. Morgan Kaufmann.
2. Hennessy, J. L., & Patterson, D. A. (2019). *Computer architecture: A quantitative approach* (6th ed.). Morgan Kaufmann.
3. Mahadevan, R. (2023). *System-on-chip architectures and interconnects*. Wiley.
4. Bhasker, J. (2021). *A SystemC primer* (3rd ed.). Star Galaxy Publishing.
5. Smith, M. J. S. (2020). *Application-specific integrated circuits*. Pearson Education.

3. E-Resources

1. RISC-V International Specifications
   `https://riscv.org/technical/specifications/`
2. Industry Standard Bus Architecture Specifications
   `https://developer.arm.com/documentation/ihi0022/latest`
3. NPTEL Course: Computer Organization and Architecture
   `https://nptel.ac.in/courses/106103068`
4. System Simulator Documentation
   `http://www.gem5.org/documentation/`
5. IEEE Xplore Digital Library NoC Research Papers
   `https://ieeexplore.ieee.org/browse/standards/topic/network-on-chip`

Industrial Relevance

This course bridges academic theory and industrial practice by focusing on the architectural bottlenecks inherent in modern System-on-Chip design. By covering standard bus protocols and network-on-chip topologies, students gain direct exposure to the interconnect frameworks utilized by global semiconductor leaders. This knowledge is critical for professional roles in front-end SoC design, verification, and performance modeling within the semiconductor industry.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	1	1	-	1	-	-	-	-	-	1	1	1	1
CO2	3	2	2	1	2	-	-	-	-	-	2	2	2	2
CO3	3	3	2	2	2	-	-	-	-	-	2	3	2	2
CO4	2	1	2	-	2	-	-	-	-	-	1	2	2	2
CO5	3	3	3	2	3	1	-	-	-	-	2	3	3	3
Weighted Average	2.60	2.00	2.00	1.67	2.00	1.00	-	-	-	-	1.60	2.20	2.00	2.00

Course Code: U23EVT09
Course Title: Semiconductor Manufacturing Technology
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
Prerequisite(s): CMOS Integrated Circuits, Electronic Devices and Circuits
SDG: 7,9,12

Course Overview

This course provides a comprehensive exploration of semiconductor manufacturing processes, ranging from raw wafer preparation to advanced fabrication, testing, and packaging. It examines the integration of various thin-film, lithography, and etching techniques to realize complex integrated circuits within high-volume production environments. The course prepares students for professional roles by establishing foundational knowledge in process engineering, quality management, and reliability assessment in the semiconductor industry.

Course Objectives

1. Analyze semiconductor material properties, wafer preparation techniques, and cleanroom operational standards required for integrated circuit manufacturing.
2. Evaluate the methodologies of CMOS process integration, including lithography, thin-film deposition, and etching sequences utilized in modern fabrication.
3. Assess semiconductor testing strategies, yield optimization techniques, reliability testing protocols, and industrial quality management frameworks.

Unit I: Semiconductor Materials and Wafer Preparation **9 Hours**
Semiconductor material properties-Silicon and compound semiconductor materials-Crystal structure and wafer orientation-Czochralski crystal growth-Wafer slicing-Lapping and polishing-Epitaxial growth-Float-zone crystal growth-Silicon-on-insulator technology.
Active Learning Activity: Prepare a process flow chart illustrating semiconductor wafer manufacturing from crystal growth to polished wafers.
Unit II: Cleanroom Technology and Thin Film Processes **9 Hours**
Cleanroom classifications and standards-Contamination control techniques-Wafer cleaning methods-RCA cleaning process-Thermal oxidation-Dry and wet oxidation-Thin film fundamentals-Physical vapor deposition-Chemical vapor deposition and atomic layer deposition.
Active Learning Activity: Develop a contamination control strategy for a semiconductor fabrication facility and evaluate its impact on manufacturing yield.
Unit III: Lithography, Etching and CMOS Process Integration **9 Hours**
Photolithography process flow-Photoresist materials-Mask generation-Optical lithography-Deep UV lithography-Reactive ion etching-Wet and dry etching-Plasma etching-CMOS process flow and multi-level metallization.
Active Learning Activity: Illustrate the fabrication sequence of a CMOS inverter showing major process steps and layer formation.
Unit IV: Semiconductor Testing and Characterization **9 Hours**
Need for semiconductor testing-Wafer probing-Probe cards-Wafer sort testing-Parametric and functional testing-Automatic test equipment overview-Electrical characterization-Process monitoring-Failure mechanisms in manufacturing.
Active Learning Activity: Analyze sample wafer test data and identify manufacturing defects affecting device performance.

Unit V: Yield Engineering, Package Flow and Quality Management **9 Hours**
Yield fundamentals-Defect density and yield models-Process variation-Statistical process control-Manufacturing quality control-Reliability testing-Semiconductor package flow-Package testing fundamentals-Technology roadmap and manufacturing trends.
Active Learning Activity: Analyze manufacturing yield reports and package test data to identify quality improvement opportunities in semiconductor production.

Course Outcomes (COs)

CO1: Explain semiconductor materials, wafer preparation techniques, and fabrication processes used in semiconductor manufacturing. (K3)

CO2: Describe cleanroom operations, oxidation, and thin-film deposition techniques employed in semiconductor fabrication. (K3)

CO3: Apply lithography, etching, implantation, metallization, and CMOS process integration concepts in semiconductor manufacturing. (K3)

CO4: Analyze semiconductor testing methodologies and identify manufacturing defects using characterization and process monitoring techniques. (K4)

CO5: Evaluate yield engineering, package flow, reliability, and quality management practices used in modern semiconductor industries. (K4)

Resources

1. Text Books

1. Plummer, J. D., Deal, M. D., & Griffin, P. B. (2024). Silicon VLSI Technology: Fundamentals, Practice and Modeling. Pearson.
2. Campbell, S. A. (2023). The Science and Engineering of Microelectronic Fabrication. Oxford University Press.
3. El-Kareh, B. (2022). Fundamentals of Semiconductor Manufacturing and Process Control. Springer.
4. Quirk, M., & Serda, J. (2021). Semiconductor Manufacturing Technology. Prentice Hall.
5. Jaeger, R. C. (2020). Introduction to Microelectronic Fabrication. Pearson.

2. Reference Books

1. Sze, S. M., & Ng, K. K. (2022). Physics of Semiconductor Devices. Wiley.
2. May, G. S., & Sze, S. M. (2021). Fundamentals of Semiconductor Fabrication. Wiley.
3. Chang, C. Y., & Sze, S. M. (2020). ULSI Technology. McGraw-Hill.
4. Rabaey, J. M., et al. (2023). Digital Integrated Circuits: A Design Perspective. Pearson.
5. Madou, M. J. (2022). Fundamentals of Microfabrication and Nanotechnology. CRC Press.

3. E-Resources

1. SEMI Standards: Guidelines for equipment and materials.
   `https://www.semi.org/en/industry-legal/standards`
2. MIT OpenCourseWare: Microelectronic Devices and circuits.
   `https://ocw.mit.edu`
3. Semiconductor Manufacturing Guide: Process fundamentals.
   `https://www.lamresearch.com`
4. NPTEL: Course on Semiconductor Devices and Circuits.
   `https://nptel.ac.in`
5. IEEE Electron Devices Society: Research and technology trends.
   `https://eds.ieee.org`

Industrial Relevance

This course bridges semiconductor device theory and industrial manufacturing practices by focusing on wafer fabrication, process integration, testing, yield optimization, package manufacturing, reliability assessment, and quality engineering methodologies used in modern semiconductor industries. It prepares students for diverse professional roles such as Process Engineer, Integration Engineer, Yield Engineer, Manufacturing Engineer, Product Engineer, Test Engineer, Packaging Engineer, and Quality Engineer in semiconductor foundries, IDMs, and OSAT industries.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	1	-	-	-	1	-	-	-	-	1	1	3	1
CO2	2	1	1	-	1	1	-	-	-	-	1	1	3	1
CO3	3	2	2	1	2	1	-	1	-	-	2	2	3	2
CO4	3	3	2	3	3	1	-	1	1	1	2	3	3	2
CO5	3	3	2	2	2	2	1	1	1	2	2	2	3	3
Weighted Average	2.60	2.00	1.40	1.20	1.60	1.20	1.00	1.00	1.00	1.00	1.60	1.80	3.00	1.80

Course Code: U23EVT10
Course Title: SoC Design I: RTL Design and Verification
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design, SystemVerilog
SDG: 9

Course Overview

This course introduces the complete front-end System-on-Chip (SoC) design flow from system specification to synthesized gate-level netlist. Students learn industry-standard RTL design methodologies, SystemVerilog coding practices, functional verification, logic synthesis, static timing analysis, and RTL quality assurance to produce implementation-ready designs for physical design.

Course Objectives

1. Explain the complete front-end SoC design flow from system specification to synthesized gate-level netlist.
2. Design synthesizable RTL modules using SystemVerilog following industry coding methodologies.
3. Apply functional verification, logic synthesis, timing analysis, and RTL sign-off methodologies to produce implementation-ready digital designs.

Unit I: SoC Design Flow and RTL Methodology **9 Hours**
Semiconductor Industry Overview - ASIC, FPGA and SoC Design Flow - Front-End and Back-End Design Methodologies - Product Development Cycle and Design Hierarchy - Functional Specifications and Design Requirements - Embedded SoC Architecture Fundamentals - RTL Abstraction Levels - Design Partitioning Methodologies - Hardware–Software Co-design Concepts - IP Reuse and IP Integration - Behavioral Synthesis (Overview) - EDA Design Environment
Active Learning Activity: Analyze a digital system specification and derive the RTL architecture, module hierarchy, and design partitioning.

Unit II: RTL Design Using SystemVerilog **9 Hours**
RTL Coding Guidelines - Hierarchical RTL Design - Combinational and Sequential Circuit Design - Finite State Machine (FSM) Design - Datapath and Controller Design - Parameterized RTL Design - Register File Architecture - FIFO Design - Memory Interface Concepts - Basic AMBA Bus Interface Concepts - RTL Simulation and Debugging - Coding for Synthesis (Best Practices)
Active Learning Activity: Design, simulate, and verify an FSM or parameterized FIFO using SystemVerilog.

Unit III: Logic Synthesis and Timing Analysis **9 Hours**
RTL Simulation Review - Logic Synthesis Fundamentals - Design Elaboration and Library Linking - Standard Cell and Technology Libraries - Logic Optimization - Technology Mapping and Gate-Level Netlist Generation - Synthesis Constraints (SDC) - Static Timing Analysis (STA) and Critical Path Analysis - Formal Equivalence Checking (Overview) - Synthesis Reports Interpretation.

Active Learning Activity:Perform RTL synthesis, analyze synthesis reports, optimize timing and area through logic optimization, and verify RTL-to-gate functional equivalence.

Unit IV: Functional Verification Methodology **9 Hours**
Verification Planning and Strategy - Testbench Architecture - Directed and Self-Checking Testbenches - Assertion-Based Verification (SystemVerilog Assertions) - Functional and Code Coverage - Constrained Random Verification - Introduction to Formal Verification (Property Checking and Model Checking – Overview) - Debug Methodologies.
Active Learning Activity:Develop a self-checking verification environment, write SystemVerilog Assertions (SVA), analyze verification coverage, and demonstrate formal property verification.

Unit V: RTL Quality and Front-End Sign-Off **9 Hours**
RTL Coding Standards - RTL Linting - Clock Domain Crossing (CDC) - Reset Design Methodology - Low-Power RTL Concepts - Clock Gating Fundamentals - RTL Documentation - IP Reuse Methodology - RTL Quality Metrics - Synthesis Sign-Off Reports - Front-End Design Review Checklist - Implementation-Ready Gate-Level Netlist
Active Learning Activity: Perform RTL quality review and front-end sign-off assessment using lint, synthesis, and timing reports.

Course Outcomes (COs)

CO1: Describe the complete front-end SoC design flow and various design methodologies (K2).

CO2: Develop synthesizable RTL modules using SystemVerilog following industry coding practices (K3).

CO3: Perform logic synthesis and static timing analysis to achieve design constraints (K3).

CO4: Design and implement comprehensive verification environments for complex digital systems (K4).

CO5: Evaluate RTL quality and execute front-end sign-off procedures for implementation-ready designs (K4).

Resources

Text Books

1. Saurabh, S. (2023). *Introduction to VLSI Design*. Cambridge University Press.
2. Sutherland, S., Davidmann, S., & Flake, P. (2021). *SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling* (3rd ed.). Springer.
3. Spear, C., & Tumbush, G. (2023). *SystemVerilog for Verification: A Guide to Learning the Testbench Language Features* (4th ed.). Springer.
4. Keating, M., Flynn, D., Aitken, R., Gibbons, A., & Shi, K. (2020). *Reuse Methodology Manual for System-on-a-Chip Designs* (3rd ed.). Springer.
5. Bhatnagar, H. (2018). *Advanced ASIC Chip Synthesis: Using Synopsys Design Compiler, Physical Compiler and PrimeTime*. Springer.

Reference Books

1. Navabi, Z., Digital Design and Verilog HDL Fundamentals, McGraw-Hill Education, 2020.
2. Thomas, D.E., and Moorby, P.R., The Verilog Hardware Description Language, Springer, 2021.
3. Bhasker, J., A SystemVerilog Primer, Star Galaxy Publishing, 2022.
4. Smith, M.J.S., Application-Specific Integrated Circuits, Pearson, 2023.
5. Bergeron, J., Writing Testbenches: Functional Verification of HDL Models, Springer, 2020.

E-Resources

1. Saurabh, S. (n.d.). *Introduction to VLSI Design*. National Programme on Technology Enhanced Learning (NPTEL), IIT Kharagpur. Available at: `https://nptel.ac.in`
2. Accellera Systems Initiative. (n.d.). *SystemVerilog Standards*. Available at: `https://www.accellera.org/downloads/standards/systemverilog`
3. IEEE. (n.d.). *IEEE Xplore Digital Library – VLSI, ASIC and SoC Design Resources*. Available at: `https://ieeexplore.ieee.org`
4. ASIC World. (n.d.). *RTL Design, Verilog and SystemVerilog Tutorials*. Available at: `https://www.asic-world.com`
5. Siemens EDA. (n.d.). *Verification Academy – SystemVerilog and UVM Learning Resources*. Available at: `https://verificationacademy.com`
6. OpenCores. (n.d.). *Open Source Hardware IP Cores and SoC Projects*. Available at: `https://opencores.org`

Industrial Relevance

This course serves as the critical bridge between theoretical digital logic and the high-stakes environment of global semiconductor product development. By mastering the industry-standard front-end design flow—including RTL coding, synthesis, and verification—students transition from academic circuit analysis to the professional practice of building silicon-ready IP. The emphasis on quality metrics, timing sign-off, and low-power methodologies directly reflects the rigorous requirements of modern SoC development, preparing graduates to contribute immediately to design and verification teams within the semiconductor industry.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	1	1	-	1	1	-	-	1	-	1	2	2	1
CO2	3	2	2	1	3	-	-	1	1	-	2	3	3	2
CO3	3	3	2	2	3	-	-	1	1	1	2	3	3	2
CO4	3	3	3	3	3	1	-	2	2	1	2	3	3	3
CO5	3	3	3	3	3	1	1	2	2	2	2	3	3	3
Weighted Average	2.80	2.40	2.20	2.25	2.60	1.00	1.00	1.50	1.40	1.33	1.80	2.80	2.80	2.20

Course Code: U23EVP05
Course Title: Digital Signal Processing Laboratory
Course Type: Professional Core Laboratory
L T P C: 0 0 4 2
Total Hours: 60
Prerequisite(s): Digital System Design
SDG: 9

Course Overview

This laboratory course is designed to provide practical experience in the algorithmic implementation, mathematical analysis, and hardware realization of digital signal processing algorithms using general-purpose computing and Hardware Description Language (HDL) simulation tools. Students develop critical hands-on skills in signal generation, system characterization, transform-domain analysis, digital filter design, finite word-length error analysis, and Register Transfer Level (RTL) functional verification. These analytical and practical competencies are directly relevant to solving complex engineering problems in the semiconductor, modern wireless communication, embedded systems, and VLSI design industries.

Course Objectives

1. To analyze and visualize discrete-time signals, linear time-invariant system properties, and transform-domain representations using open-source academic simulation tools.
2. To design, realize, and evaluate Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) digital filters to meet specific frequency response specifications.
3. To investigate fixed-point quantization effects and perform Register Transfer Level (RTL) modeling and functional verification of digital signal processing blocks for VLSI architectures.

Laboratory Experiments

Experiment 1: Generation and Visualization of Fundamental Discrete-Time Signals (CO1)
Generate and visualize standard discrete-time test signals including unit impulse, unit step, unit ramp, exponential, and sinusoidal sequences using open-source academic simulation tools.

Experiment 2: Analysis of LTI System Properties: Linearity, Causality, and Stability (CO1)
Evaluate and verify the core properties of Discrete-Time Linear Time-Invariant (LTI) systems, specifically testing for linearity, time-invariance, causality, and bounded-input bounded-output (BIBO) stability through numerical simulation.

Experiment 3: Sampling Theorem Verification and Aliasing Analysis (CO2)
Verify the Nyquist-Shannon sampling theorem by sampling continuous-time bandlimited signals at various sampling rates and analyzing the resulting spectral aliasing effects in the frequency domain.

Experiment 4: Z-Transform Analysis and System Response Characterization (CO2)
Compute the Z-transform of discrete-time sequences, plot pole-zero configurations in the Z-

plane, and determine the system impulse response and frequency response characterization.

Experiment 5: Linear and Circular Convolution using DFT (CO3)
Perform linear and circular convolution of discrete-time sequences using the Discrete Fourier Transform (DFT) and Inverse Discrete Fourier Transform (IDFT), verifying time-domain and frequency-domain equivalence.

Experiment 6: Radix-2 FFT Algorithm Implementation and Complexity Evaluation (CO3)
Implement decimation-in-time and decimation-in-frequency Radix-2 Fast Fourier Transform (FFT) algorithms and evaluate their computational complexity against direct Discrete Fourier Transform computation.

Experiment 7: Design and Realization of FIR Filters using Window Techniques (CO4)
Design and realize linear-phase Finite Impulse Response (FIR) low-pass, high-pass, band-pass, and band-stop filters using standard window techniques including Rectangular, Hamming, Hanning, and Blackman windows.

Experiment 8: Design and Realization of IIR Filters using Bilinear Transformation (CO4)
Design and realize Infinite Impulse Response (IIR) Butterworth and Chebyshev digital filters from analog prototypes utilizing the Bilinear Transformation method and verify their magnitude and phase responses.

Experiment 9: Fixed-Point Arithmetic and Quantization Error Analysis (CO5)
Simulate fixed-point arithmetic operations, model finite word-length effects, and analyze quantization errors and coefficient quantization impacts on filter frequency response and system stability.

Experiment 10: RTL Modeling and Functional Verification of an FIR Filter (CO5)
Develop a Register Transfer Level (RTL) model of a Finite Impulse Response (FIR) filter using a hardware description language and perform comprehensive functional verification using testbenches in an open-source HDL simulator.

Course Outcomes

Upon completion of this laboratory course, the students will be able to:

CO1: Analyze fundamental discrete-time signals and evaluate the linearity, causality, and stability properties of Linear Time-Invariant (LTI) systems. (K4)

CO2: Analyze the sampling theorem, spectral aliasing, and system response characteristics using Z-transform representations in the frequency domain. (K4)

CO3: Apply Discrete Fourier Transform (DFT) and Radix-2 Fast Fourier Transform (FFT) algorithms to perform linear and circular convolution and evaluate computational complexity. (K3)

CO4: Design and realize Finite Impulse Response (FIR) using window techniques and Infinite Impulse Response (IIR) digital filters using Bilinear Transformation to meet specified frequency response criteria. (K5)

CO5: Evaluate quantization errors in fixed-point arithmetic and develop Register Transfer Level (RTL) models with functional verification for digital filter architectures. (K6)

Resources

Text Books

1. Proakis, J. G., & Manolakis, D. G. (2014). *Digital signal processing: Principles, algorithms, and applications* (4th ed.). Pearson Education.
2. Oppenheim, A. V., & Schafer, R. W. (2010). *Discrete-time signal processing* (3rd ed.). Prentice Hall.

Reference Books

1. Mitra, S. K. (2011). *Digital signal processing: A computer-based approach* (4th ed.). McGraw-Hill Education.
2. Lyons, R. G. (2011). *Understanding digital signal processing* (3rd ed.). Prentice Hall.
3. Meyer-Baese, U. (2014). *Digital signal processing with field programmable gate arrays* (4th ed.). Springer.

E-Resources

1. Massachusetts Institute of Technology. (2023). *Discrete-time signal processing (MIT OpenCourseWare).*
   `https://ocw.mit.edu/courses/6-341-discrete-time-signal-processing-fall-2005/`
2. National Programme on Technology Enhanced Learning. (2023). *Digital signal processing and its applications.*
   `https://nptel.ac.in/courses/117102060`
3. GNU Project. (2024). *GNU Octave: Scientific programming language for signal processing.*
   `https://www.gnu.org/software/octave/`
4. Icarus Verilog & GTKWave. (2024). *Open-source HDL simulation and waveform verification tools.*
   `https://steveicarus.github.io/iverilog/`
5. Scilab Enterprises. (2024). *Scilab: Open source software for numerical computation and signal processing.*
   `https://www.scilab.org/`

Industrial Relevance

This laboratory course significantly enhances students' measurement skills, instrumentation skills, hardware implementation skills, communication system testing, circuit debugging, and validation and verification techniques by bridging theoretical digital signal processing concepts with practical VLSI hardware realizations. Through rigorous simulation and algorithmic modeling using open-source academic tools, students learn to measure and analyze spectral characteristics, quantify finite word-length and quantization noise, and debug complex signal flow graphs. Furthermore, the transition from algorithmic design to Register Transfer Level (RTL) modeling and testbench-driven functional verification instills industry-standard verification techniques

essential for identifying timing and logic anomalies. These comprehensive practical competencies are directly transferable and critically relevant to the semiconductor, communication, embedded systems, and VLSI industries, where engineers design, verify, and optimize high-speed Application-Specific Integrated Circuits (ASICs), Field-Programmable Gate Arrays (FPGAs), and System-on-Chip (SoC) architectures for next-generation telecommunications and edge-computing applications.

CO–PO–PSO Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	3	3	–	–	3	3	–	2	3	3	2
CO2	3	3	2	3	3	–	–	3	3	–	2	3	3	2
CO3	3	2	3	3	3	–	–	3	3	–	3	3	3	2
CO4	3	3	3	3	3	–	–	3	3	2	3	3	3	3
CO5	3	3	3	3	3	–	1	3	3	2	3	3	3	3
Weighted Average	**3.00**	**2.80**	**2.60**	**3.00**	**3.00**	**–**	**1.00**	**3.00**	**3.00**	**2.00**	**2.60**	**3.00**	**3.00**	**2.40**

Course Code: U23EVP06
Course Title: RTL Design and Verification Laboratory
Course Type: Professional Core Laboratory
L T P C: 0 0 4 2
Total Hours: 60
SDG: 9

Course Overview

This laboratory course provides comprehensive exposure to the front-end VLSI design and verification flow, bridging digital system specifications with implementation-ready RTL designs. Students gain hands-on experience in hardware description language-based RTL development, logic synthesis, timing constraint application, static timing analysis, verification methodologies, and RTL sign-off practices. The course emphasizes industry-standard design and verification workflows widely adopted in semiconductor product development.

Course Objectives

1. To explain the complete front-end ASIC/SoC design flow from specification to RTL sign-off.
2. To design synthesizable hardware description language RTL modules using modular and reusable design methodologies.
3. To apply logic synthesis, timing constraints, verification techniques, and RTL quality assessment for implementation readiness.

Laboratory Experiments

Experiment 1: ASIC Design Flow Environment Setup (CO1)
Configure the EDA design environment, practice Linux shell commands, and manage project directories for ASIC design workflows.
Experiment 2: RTL Architecture and Module Partitioning (CO1)
Analyze a digital system specification, develop RTL architecture, and establish module hierarchy and interfaces.
Experiment 3: Combinational and Sequential RTL Design (CO2)
Design, implement, and simulate combinational logic circuits, sequential circuits, and finite state machine (FSM) based controllers.
Experiment 4: Parameterized RTL Design and Memory Modeling (CO2)
Develop parameterized RTL modules and model FIFO, SRAM, and ROM-based memory interfaces.
Experiment 5: Logic Synthesis Fundamentals (CO3)
Perform logic synthesis of RTL modules using standard-cell libraries and generate gate-level netlists.
Experiment 6: Timing Constraints and Static Timing Analysis (CO3)
Apply constraints including clocks, input/output delays, and analyze timing reports to identify critical paths.
Experiment 7: Self-Checking Testbench Development (CO4)
Develop self-checking testbenches to automate functional verification of RTL modules.

Experiment 8: Assertion-Based Verification and Functional Coverage (CO4)
Develop verification environments utilizing assertions and functional coverage to evaluate verification completeness.
Experiment 9: RTL Coding Standards and Lint Analysis (CO5)
Perform RTL quality assessment through coding standard compliance checks and lint analysis.
Experiment 10: RTL Sign-Off and Implementation Readiness Assessment (CO5)
Conduct RTL sign-off assessment, review synthesis, timing and verification reports, evaluate design quality metrics, and prepare implementation-ready design documentation.

Course Outcomes

CO1: Explain ASIC/SoC front-end design flow, RTL methodologies, and implementation processes. (K2)
CO2: Design synthesizable RTL modules including combinational logic, sequential logic, FSMs, FIFOs, and memory interfaces. (K3)
CO3: Apply logic synthesis, timing constraints, and static timing analysis techniques for gate-level implementation. (K3)
CO4: Develop verification environments using self-checking testbenches, assertions, and functional coverage methodologies. (K3)
CO5: Analyze RTL quality, perform sign-off reviews, and prepare implementation-ready design documentation. (K4)

Resources

Text Books

1. Stuart Sutherland, "System Verilog for Design: A Guide to Using System Verilog for Hardware Design and Modeling," Springer, 2020.
2. Chris Spear and Greg Tumbush, "SystemVerilog for Verification: A Guide to Learning the Testbench Language Features," Springer, 2022.
3. Micheal John Sebastian Smith, "Application-Specific Integrated Circuits," Addison-Wesley, 2021 (Reprint).
4. Simon Davidmann and Ray Salemi, "System Verilog for Verification," 3rd Ed., Springer, 2023.
5. Donald Thomas and Philip Moorby, "The Verilog Hardware Description Language," Springer, 2024.

Reference Books

1. Ben Cohen, "System Verilog Assertions Handbook," VhdlCohen Publishing, 2020.
2. Janick Bergeron, "Writing Testbenches using System Verilog," Springer, 2021.
3. Ashok B. Mehta, "Digital Design with Verilog," Elsevier, 2022.
4. Zainalabedin Navabi, "Digital System Design with System Verilog," McGraw-Hill Education, 2023.
5. Douglas L. Perry, "Verilog HDL: A Guide to Digital Design and Synthesis," McGraw-Hill, 2025.

E-Resources

1. `https://www.accellera.org`
2. `https://verificationguide.com`
3. `https://www.asic-world.com`

4. `https://nptel.ac.in/courses/106105161`
5. `https://www.edaplayground.com`

Industrial Relevance

This laboratory develops essential practical competencies in measurement, instrumentation, and hardware implementation, directly mapping to the rigorous demands of the semiconductor, communication, embedded systems, and VLSI industries. By engaging in circuit debugging, design validation, and comprehensive verification techniques, students master the full front-end development cycle. These skills ensure graduates can execute complex tasks such as RTL sign-off and timing closure, making them highly effective contributors in modern product development teams and advanced engineering research environments.

CO–PO–PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	1	2	2	1	-	1	1	-	1	2	2	1
CO2	2	2	3	2	3	-	-	2	2	-	2	3	2	2
CO3	2	2	2	3	3	-	-	2	2	-	2	3	3	2
CO4	2	3	3	3	3	-	-	2	2	-	2	3	3	2
CO5	2	3	2	3	3	1	-	2	3	1	2	3	3	3
Weighted Average	2.00	2.40	2.20	2.60	2.80	1.00	-	1.80	2.00	1.00	1.80	2.80	2.60	2.00

Course Code: U23EVT11
Course Title: Embedded Systems Architecture and Design
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design; Computer Architecture and On-Chip Communication
SDG: 7,9,11

Course Overview

This course introduces the architecture, programming and design principles of modern embedded systems. It covers ARM Cortex-M and RISC-V processor architectures, Embedded C programming, memory organization, peripheral interfacing, real-time operating systems, firmware development and hardware–software integration. The course develops practical skills in designing, debugging and integrating embedded systems for IoT, automotive, industrial and edge-computing applications.

Course Objectives

1. Explain embedded processor architectures, instruction-set fundamentals, memory organization and development environments of ARM Cortex-M and RISC-V processors.
2. Develop Embedded C programs and real-time applications involving memory, interrupts and peripheral interfaces.
3. Apply hardware–software co-design, firmware development, device-driver, debugging and system-integration techniques in embedded system development.

Unit I: Introduction to Embedded Systems and Processor Architecture 9 Hours
Introduction to Embedded Systems – Characteristics and Classification of Embedded Systems – Embedded System Design Flow – Hardware and Software Components – Microcontroller and Microprocessor Architectures – ARM Cortex-M Architecture Overview – RISC-V Architecture Overview – RISC-V Instruction Set Architecture Fundamentals – Processor and Memory Organization – Embedded Development Toolchain – Cross-Compilation Process.
Active Learning Activity: Develop and simulate a simple embedded application using an ARM Cortex-M or open-source RISC-V development environment.

Unit II: Embedded Programming and Peripheral Interfacing 9 Hours
Embedded C Programming Fundamentals – Memory Organization – Memory Mapping – GPIO Programming – Timers and Counters – Interrupt Handling – Interrupt Service Routines – UART Communication – SPI Communication – I²C Communication – Introduction to DMA – Peripheral Configuration and Data Transfer.
Active Learning Activity: Develop Embedded C programs for peripheral interfacing using GPIO, UART, SPI or I²C on a simulation environment or development board.

Unit III: Real-Time Operating Systems 9 Hours
Introduction to Real-Time Systems – Characteristics of Real-Time Systems – Hard and Soft Real-Time Systems – RTOS Architecture – Tasks and Threads – Task States – Scheduling Techniques – Context Switching – Inter-Task Communication – Semaphores – Mutex – Message Queues – Software Timers – Introduction to FreeRTOS – Real-Time Application Development.

Active Learning Activity: Develop a multitasking embedded application using FreeRTOS and analyze task scheduling and synchronization.

Unit IV: Hardware–Software Co-Design and Firmware Development **9 Hours**
Hardware–Software Co-Design Concepts – Hardware–Software Partitioning – Co-Design Methodology – Embedded Firmware Development Process – Board Support Package (BSP) – Hardware Abstraction Layer (HAL) – Device Driver Fundamentals – Memory-Mapped Peripheral Interface – Firmware–Hardware Interaction – Firmware Testing – Embedded Debugging Techniques – JTAG and SWD Basics – Integrated Development Environment (IDE) – Build and Debug Process.
Active Learning Activity: Develop, debug and validate firmware for a hardware peripheral using an embedded development environment.

Unit V: Secure Embedded SoC Applications **9 Hours**
Embedded System Integration – Processor, Memory and Peripheral Integration – Embedded System Performance and Reliability – Embedded System Development and Deployment – IoT Embedded Systems – Automotive Embedded Systems – Industrial Embedded Systems – Edge Embedded Applications – Embedded System Platforms – Embedded System Case Studies.
Active Learning Activity: Analyze an embedded-system case study and identify the processor, memory, peripherals, firmware and hardware–software interaction.

Course Outcomes

Upon successful completion of the course, students will be able to:

CO1: Explain embedded processor architectures, instruction-set fundamentals, memory organization and development environments of ARM Cortex-M and RISC-V processors. (K2)

CO2: Apply Embedded C programming and peripheral interfacing techniques using GPIO, timers, interrupts, UART, SPI, I²C and DMA. (K3)

CO3: Implement real-time embedded applications using RTOS concepts including task scheduling, synchronization and inter-task communication. (K3)

CO4: Apply hardware–software co-design, firmware development, device-driver, testing and debugging techniques in embedded systems. (K3)

CO5: Analyze the integration and application of embedded systems in IoT, automotive, industrial and edge-computing domains. (K4)

Resources

1. Text Books

1. Shibu, K. V. (2020). *Introduction to embedded systems* (3rd ed.). McGraw Hill Education.
2. Vahid, F., & Givargis, T. (2021). *Embedded system design: A unified hardware/software introduction* (3rd ed.). Wiley.
3. Valvano, J. W. (2020). *Embedded systems: Introduction to ARM Cortex-M microcontrollers* (5th ed.). CreateSpace Independent Publishing.
4. Amos, B. (2020). *Hands-On RTOS with microcontrollers: Building real-time embedded systems.* Packt Publishing.

5. Patterson, D. A., & Hennessy, J. L. (2020). *Computer organization and design: RISC-V edition: The hardware software interface* (2nd ed.). Morgan Kaufmann.

2. Reference Books

1. Kamal, R. (2023). *Embedded systems: Architecture, programming and design* (4th ed.). McGraw Hill Education.
2. Lee, E. A., & Seshia, S. A. (2019). *Introduction to embedded systems: A cyber-physical systems approach* (2nd ed.). MIT Press.
3. Ledin, J. (2021). *Architecting high-performance embedded systems*. Packt Publishing.
4. Walls, C. (2020). *Embedded software: The works* (3rd ed.). Newnes.
5. Zhu, Y. (2019). *Embedded systems with ARM Cortex-M microcontrollers in assembly language and C* (3rd ed.). E-Man Press.

3. E-Resources

1. NPTEL. (2021). *Embedded systems design*. Note: Covers processor architectures, memory mapping, and hardware-software co-design fundamentals.
`https://nptel.ac.in/courses/108102045`
2. RISC-V International. (2022). *RISC-V instruction set manual: Volume I - Unprivileged architecture*. Note: Comprehensive architectural specifications and instruction set details for RISC-V processors.
`https://riscv.org/technical/specifications/`
3. FreeRTOS. (2021). *FreeRTOS real-time kernel reference manual*. Note: Practical guide on kernel architecture, task scheduling, semaphores, and memory management in real-time operating systems.
`https://www.freertos.org/RTOS-kernel-reference-manual.html`
4. ARM Developer. (2020). *Cortex-M generic user guide*. Note: Technical documentation detailing core architecture, register configurations, and programming models for embedded developers.
`https://developer.arm.com/documentation/`
5. NPTEL. (2022). *Real-time operating systems*. Note: In-depth analysis of deterministic scheduling, priority inversion, and task communication in modern embedded environments.
`https://nptel.ac.in/courses/106105172`

Industrial Relevance

This course bridges the gap between academic theory and global semiconductor industrial practices by providing a comprehensive, hands-on framework for embedded system engineering on modern System-on-Chip (SoC) architectures. In contemporary semiconductor fabrication, automotive engineering, consumer electronics, and industrial automation, professionals must adeptly navigate the co-design of hardware peripherals and low-level firmware. By mastering industry-standard processor architectures such as ARM Cortex-M and open-source RISC-V, alongside real-time operating system (RTOS) deterministic scheduling, device driver development, and secure boot implementations, graduates are equipped to address critical challenges in low-power optimization and hardware security. This curriculum ensures immediate technical relevance,

enabling future VLSI and embedded engineers to seamlessly transition into roles involving SoC validation, firmware architecture, and intelligent IoT systems development across leading global technology enterprises.

CO-PO-PSO Articulation Matrix

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	-	2	-	-	-	-	-	2	3	2	2
CO2	3	2	3	2	3	-	-	-	-	-	2	3	3	2
CO3	3	3	3	2	3	1	-	2	-	-	2	3	3	2
CO4	3	3	3	3	3	2	-	2	2	1	3	3	3	3
CO5	3	3	3	3	2	3	2	2	2	2	3	3	3	3
Weighted Average	3.00	2.60	2.60	2.50	2.60	2.00	2.00	2.00	2.00	1.50	2.40	3.00	2.80	2.40

Course Code: U23EVT12
Course Title: VLSI Testing and Validation
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design; SoC Design I: RTL Design and Verification
SDG: 9,12

Course Overview

This professional core course provides a rigorous exploration of the principles, architectural methodologies, and industrial workflows essential for the testing, validation, and quality qualification of modern digital integrated circuits and System-on-Chip (SoC) devices. Key themes encompass structural fault modeling, scan-based Design-for-Testability (DFT) architectures, Automatic Test Pattern Generation (ATPG) algorithms, memory and logic Built-In Self-Test (BIST) structures, and boundary scan standards. By bridging theoretical test concepts with pre-silicon and post-silicon validation workflows, the course equips students with vital engineering competencies required for careers in DFT methodologies, product characterization, yield optimization, and semiconductor manufacturing.

Course Objectives

1. To analyze fundamental semiconductor failure mechanisms, structural fault models, and quality metrics to establish robust test specifications for VLSI systems.
2. To design and implement advanced Design-for-Testability (DFT) architectures, including scan chains, memory BIST, and boundary scan structures, optimizing circuit controllability and observability.
3. To evaluate Automatic Test Pattern Generation (ATPG) workflows, fault coverage reports, and post-silicon validation methodologies across the semiconductor product lifecycle.

Unit I: Fundamentals of IC Testing **9 Hours**
Introduction to Semiconductor Testing – Manufacturing Defects and Failure Mechanisms – Need for Testing – Defect Level – Quality Metrics – Yield and Reliability Concepts – Functional Testing and Structural Testing – Fault Models – Stuck-at Faults – Bridging Faults – Open Faults – Delay Faults – Fault Equivalence – Fault Dominance – Fault Collapsing – Test Challenges in Modern SoCs.
Active Learning Activity: Analyze manufacturing defects in a digital circuit and identify suitable fault models for structural testing using vendor-neutral open-source simulation environments.

Unit II: Design for Testability (DFT) **9 Hours**
Testability Concepts – Controllability and Observability – Design-for-Testability Principles – Scan Cell Architecture – Full Scan and Partial Scan Methodologies – Scan Chain Design – Scan Chain Verification – Test Modes – Test Compression Concepts – Embedded Deterministic Test (EDT) (Introduction) – DFT Coding Guidelines – DFT Planning for SoCs – Introduction to Industrial DFT Flow.
Active Learning Activity: Develop a scan-enabled RTL design and evaluate improvements in controllability and observability through automated structural rule checking.

Unit III: Automatic Test Pattern Generation (ATPG) **9 Hours**
Introduction to ATPG – ATPG Flow – Combinational and Sequential Fault Simulation – Stuck-at Fault ATPG – Transition Fault ATPG – Pattern Generation – Pattern Verification – Fault Coverage Metrics – Coverage Reports – Test Quality Evaluation – Industrial ATPG Flow – Introduction to Advanced Industrial ATPG Methodology.
Active Learning Activity: Generate test patterns for a scan-based digital circuit and evaluate fault coverage metrics using industry-standard ATPG coverage reports.

Unit IV: Embedded Test Techniques **9 Hours**
Memory Fault Models – Memory Testing Fundamentals – March Algorithms – Memory Built-In Self-Test (MBIST) – Logic Built-In Self-Test (LBIST) – Linear Feedback Shift Register (LFSR) – Multiple Input Signature Register (MISR) – Boundary Scan Architecture – IEEE 1149.1 (JTAG) – Embedded Test Architectures – On-Chip Test Structures.
Active Learning Activity: Design a basic MBIST architecture and analyze memory fault detection using March algorithms within a verification testbench.

Unit V: Silicon Validation and Product Engineering **9 Hours**
Industrial Test Flow from RTL to Production Testing – Scan Insertion Overview – Pre-Silicon Validation – Post-Silicon Validation – Wafer Probe Testing – Package Testing – Burn-In Testing – Product Characterization – Yield Analysis Fundamentals – Failure Analysis – Semiconductor Test Equipment – Reliability Qualification – Product Engineering Workflow – Overview of Industrial DFT Tools.
Active Learning Activity: Study the complete semiconductor product lifecycle and analyze testing and validation activities performed from initial RTL freeze to volume production.

Course Outcomes (COs)

After successful completion of the course, students will be able to:

CO1. Formulate structural fault models and evaluate semiconductor quality metrics, defect levels, and failure mechanisms in digital integrated circuits. (K3)

CO2. Apply Design-for-Testability (DFT) methodologies, including full and partial scan architectures, to optimize circuit controllability and observability. (K3)

CO3. Analyze Automatic Test Pattern Generation (ATPG) algorithms, fault simulation workflows, and test coverage metrics for complex digital systems. (K4)

CO4. Apply embedded test techniques, including MBIST, LBIST, and IEEE 1149.1 boundary scan architectures, for testing System-on-Chip (SoC) designs. (K3)

CO5. Analyze post-silicon validation flows, production testing methodologies, yield analysis, and reliability qualification workflows in semiconductor manufacturing. (K4)

Resources

1. Text Books

1. Wang, L.-T., Wu, C.-W., & Wen, X. (2020). *VLSI test principles and architectures: Design for testability* (2nd ed.). Morgan Kaufmann.

2. Bushnell, M. L., & Agrawal, V. D. (2022). *Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits*. Springer Nature.

3. Abramovici, M., Breuer, M. A., & Friedman, A. D. (2023). *Digital systems testing and testable design*. IEEE Press.

4. Crouch, A. L. (2021). *Design for test for digital ICs and embedded core systems*. Prentice Hall.

5. Rajski, J., & Tyszer, J. (2023). *Design for testability: The basics*. Springer Nature.

2. Reference Books

1. Wang, L.-T., et al. (2021). *System-on-chip test architectures: Nanometer design for testability*. Morgan Kaufmann.

2. Benso, A., & Prinetto, P. (2020). *Fault injection techniques and tools for embedded systems reliability evaluation*. CRC Press.

3. Koushanfar, F., & Tehranipoor, M. (2023). *Introduction to hardware security and trust*. Springer Nature.

4. Jha, N. K., & Gupta, S. (2019). *Testing of digital systems*. Cambridge University Press.

5. Stroud, C. E. (2022). *A designer's guide to built-in self-test*. Springer Science & Business Media.

3. E-Resources

1. NPTEL. (2023). *Design for testability* [Online Course]. Indian Institute of Technology Kharagpur. Note: Scan design and BIST architectures.
`https://nptel.ac.in/courses/106105161`

2. MIT OpenCourseWare. (2021). *Testing and verification of digital circuits* [Lecture Notes]. Massachusetts Institute of Technology. Note: Fault modeling and ATPG algorithms.
`https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/`

3. IEEE Standards Association. (2020). *IEEE Standard for Test Access Port and Boundary-Scan Architecture (IEEE Std 1149.1)*. Note: JTAG architecture and boundary scan instructions.
`https://standards.ieee.org/standard/1149_1-2013.html`

4. NPTEL. (2022). *VLSI physical design and testing* [Online Course]. Indian Institute of Technology Madras. Note: Silicon validation and yield analysis fundamentals.
`https://nptel.ac.in/courses/117106093`

5. OpenCores. (2023). *Open-source DFT and BIST hardware blocks* [Technical Repository]. Note: RTL implementations of LFSR, MISR, and memory BIST controllers.
`https://opencores.org/projects`

Industrial Relevance

In the contemporary semiconductor industry, where System-on-Chip (SoC) architectures integrate billions of transistors at deep sub-micron design nodes, testing and validation account for a significant portion of total product manufacturing costs and time-to-market. This course bridges academic structural theory with industrial silicon deployment by embedding

industry-standard Design-for-Testability (DFT) methodologies, Automatic Test Pattern Generation (ATPG) workflows, and embedded self-test architectures directly into the learning progression. Students transition from theoretical fault modeling to practical pre-silicon and post-silicon validation paradigms, mirroring the exact functional workflows utilized by leading fabless semiconductor design houses and integrated device manufacturers (IDMs). By addressing critical industrial challenges such as test data compression, yield optimization, automated test equipment (ATE) interfacing, and reliability qualification, the curriculum prepares graduates to seamlessly step into high-demand roles as DFT engineers, silicon validation specialists, and product engineers, directly supporting the global hardware ecosystem and advanced chip manufacturing initiatives.

CO-PO-PSO Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	-	2	-	-	-	-	-	2	3	2	-
CO2	3	3	3	-	3	-	-	-	-	-	2	3	3	2
CO3	3	3	2	3	3	-	-	-	-	-	2	3	3	2
CO4	3	2	3	-	3	-	-	-	-	-	2	3	3	2
CO5	3	3	2	3	3	2	1	-	-	-	3	3	3	3
Weighted Average	3.00	2.60	2.20	3.00	2.80	2.00	1.00	-	-	-	2.20	3.00	2.80	2.25

Course Code: U23EVT13
Course Title: SoC Design II: Physical Design and Chip Implementation
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: CMOS Integrated Circuits, SoC Design I: RTL Design and Verification SDG: 7,9,12

Course Overview

This course covers the complete ASIC physical design flow from synthesized gate-level netlist to fabrication-ready GDSII. Students learn floorplanning, placement, clock tree synthesis, routing, timing closure, physical verification, and sign-off methodologies used in modern semiconductor industries. This curriculum bridges the gap between theoretical RTL design and the physical realization of high-performance integrated circuits.

Course Objectives

1. Explain the complete ASIC physical design flow from synthesized gate-level netlist to GDSII.
2. Apply physical implementation methodologies for digital integrated circuits.
3. Analyze timing, power, congestion, manufacturability, and sign-off reports to generate fabrication-ready layouts.

Unit I: Introduction to Physical Design Flow and Design Constraints 9 Hours
Gate-Level Netlist to GDSII Flow - Front-End and Back-End Integration - Physical Design Databases - Reading Synthesized Netlist - Technology Files - Standard Cell Libraries - Liberty (.lib) - LEF - DEF - GDSII Format - Design Constraints Fundamentals - Clock, Input and Output Constraints - Physical Design Environment - Design Reports Interpretation
Active Learning Activity: Import a synthesized design and analyze technology libraries, constraints, and implementation reports.

Unit II: Floorplanning and Power Planning 9 Hours
Floorplanning Concepts - Core Utilization - Aspect Ratio - I/O Planning - Macro Placement - Hierarchical Floorplanning - Placement Blockages - Keep-Out Regions - Power Planning - Power Rings - Power Distribution Network (PDN) - Power Straps - Floorplan Optimization - Floorplan Analysis Reports
Active Learning Activity: Develop and evaluate the floorplan of a digital design containing memory macros.

Unit III: Placement and Physical Design Optimization 9 Hours
Standard Cell Placement - Timing-Driven Placement - Placement Optimization - Congestion Analysis - Wirelength Optimization - Density Optimization - Utilization Analysis - IR Drop Fundamentals - Scan Chain Reordering - Low-Power Physical Design - Power Domains - Isolation Cells - Level Shifters - Placement Quality Analysis
Active Learning Activity: Evaluate placement reports and optimize congestion, utilization, and timing.

Unit IV: Clock Tree Synthesis, Routing and Timing Closure **9 Hours**
Clock Tree Synthesis (CTS) - Clock Skew - Clock Latency - Setup and Hold Analysis - Timing Violation Fixes - Multi-Corner Multi-Mode (MCMM) Analysis - Global Routing - Detailed Routing - Routing Congestion Analysis - Signal Integrity Basics - Static Timing Analysis - Engineering Change Orders (ECO) - Timing Closure Methodology
Active Learning Activity: Analyze CTS and routing reports to resolve setup and hold violations.

Unit V: Physical Verification and Sign-Off **9 Hours**
Design Rule Checking (DRC) - Layout Versus Schematic (LVS) - Antenna Effects - Parasitic Extraction (PEX) - Metal Fill - Design for Manufacturability (DFM) - Power Integrity Overview (IR Drop and Electromigration) - Physical Design Sign-Off - Sign-Off Checklist - GDSII Generation - Tape-Out Flow - Industrial Physical Design Flow
Active Learning Activity: Review physical verification reports and complete fabrication sign-off for a sample design.

Course Outcomes (COs)

CO1: Explain the complete ASIC physical design flow from synthesized gate-level netlist to GDSII. (K2)
CO2: Apply physical implementation methodologies for digital integrated circuits. (K3)
CO3: Analyze timing, power, congestion, manufacturability, and sign-off reports to generate fabrication-ready layouts. (K4)
CO4: Interpret complex design constraints and reports to ensure silicon success. (K3)
CO5: Execute sign-off procedures including DRC, LVS, and PEX for final chip tape-out. (K3)

Resources

Text Books

1. Saurabh, S. (2024). *Introduction to VLSI design flow*. Cambridge University Press.
2. Kahng, A. B., Lienig, J., Markov, I. L., & Hu, J. (2022). *VLSI physical design: From graph partitioning to timing closure*. Springer.
3. Lim, S. K. (2021). *Physical design essentials: An ASIC design implementation perspective*. Springer.
4. Weste, N., & Harris, D. (2024). *CMOS VLSI design: A circuits and systems perspective* (5th ed.). Pearson.
5. Sze, S. M., & Lee, M. K. (2024). *Semiconductor devices: Physics and technology* (4th ed.). Wiley.

Reference Books

1. De Micheli, G. (2020). *Synthesis and optimization of digital circuits*. McGraw-Hill.
2. Smith, M. J. S. (2021). *Application-specific integrated circuits*. Pearson.
3. Baker, R. J. (2022). *CMOS: Circuit design, layout, and simulation* (4th ed.). Wiley.
4. Hodges, D. A., Jackson, H. G., & Saleh, R. E. (2021). *Analysis and design of digital integrated circuits* (4th ed.). McGraw-Hill.
5. Sanguinetti, J. (2020). *The art of hardware architecture: Design methods and techniques for digital circuits*. Springer.

E-Resources

1. OpenROAD Project Documentation
`https://openroad.readthedocs.io/`
2. IEEE Solid-State Circuits Society Resource Center
`https://sscs.ieee.org/publications/resource-center`
3. Global Semiconductor Alliance (GSA) Industry Reports
`https://www.gsaglobal.org/resources/`
4. VLSI Physical Design Tutorials and Methodology Guides
`https://vlsiphysicaldesign.com/`
5. NPTEL Online Course: Digital VLSI System Design
`https://nptel.ac.in/courses/106105161`

Industrial Relevance

This course directly mirrors the professional workflows utilized in global semiconductor foundries and design houses. By emphasizing the transition from logical synthesis to physical GDSII, the curriculum ensures that students are prepared for roles in physical implementation, timing analysis, and sign-off engineering. The focus on multi-corner multi-mode (MCMM) analysis and physical verification equips students with the specific, practical skills required to handle high-density, low-power modern system-on-chip (SoC) architectures.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	0	2	0	0	0	1	0	2	3	2	1
CO2	3	2	3	2	3	1	0	2	1	1	2	3	3	2
CO3	3	3	3	3	3	2	1	2	2	2	2	3	3	2
CO4	3	3	2	2	3	1	0	1	1	1	2	3	3	2
CO5	3	2	3	3	3	2	1	2	2	2	3	3	3	3
Weighted Average	3.00	2.40	2.40	2.50	2.80	1.50	1.00	1.75	1.40	1.50	2.20	3.00	2.80	2.00

Course Code: U23EVT14
Course Title: WIRELESS COMMUNICATION SYSTEMS
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
Prerequisite: Analog and Digital Communication
SDG: 9,11

Course Overview

This course provides a comprehensive exploration of modern wireless communication systems, establishing a rigorous foundation in radio propagation mechanisms, multipath fading channel characterization, and diversity combining techniques. It emphasizes advanced broadband transmission paradigms and multi-antenna architectures, including Orthogonal Frequency Division Multiplexing (OFDM) and Multiple-Input Multiple-Output (MIMO) configurations essential for high-capacity digital links. By bridging analytical channel modeling with contemporary cellular frameworks such as 5G New Radio and emerging 6G networks, the course equips students to design and optimize next-generation wireless systems and baseband hardware architectures.

Course Objectives

1. To analyze radio wave propagation mechanisms, empirical path loss models, and multipath fading channel characteristics across diverse wireless environments.
2. To evaluate digital communication performance over fading channels and investigate diversity combining, multicarrier OFDM transmission, and multiple-antenna MIMO techniques for enhanced link reliability and spectral efficiency.
3. To examine cellular system architectures, mobility management protocols, and emerging radio access technologies deployed in 4G LTE, 5G New Radio, and next-generation wireless networks.

Unit I: WIRELESS PROPAGATION AND CHANNEL MODELS **9 Hours**
Wireless communication environment – Radio propagation mechanisms – Reflection, diffraction and scattering – Free-space propagation – Path loss – Link budget – Log-distance path loss model – Shadowing – Multipath propagation – Delay spread – Doppler spread – Coherence bandwidth and coherence time – Small-scale fading – Flat and frequency-selective fading – Slow and fast fading – Rayleigh and Rician fading models.
Active Learning Activity: Analysis of path loss and multipath fading characteristics for indoor and outdoor wireless environments using system-level numerical simulation tools.

Unit II: FADING CHANNELS AND DIVERSITY TECHNIQUES **9 Hours**
Performance of digital signals over fading channels – Outage probability – Average error probability concepts – Inter-Symbol Interference in multipath channels – Equalization principles – Linear equalization – Adaptive equalization concepts – Diversity principles – Time, frequency and spatial diversity – Selection combining – Equal gain combining – Maximum ratio combining – Transmit diversity – Space-Time Block Coding – Adaptive modulation concepts.
Active Learning Activity: Comparative simulation analysis of various diversity combining techniques over Rayleigh and Rician fading channels using open-source communication modeling frameworks.

Unit III: MULTICARRIER AND OFDM SYSTEMS **9 Hours**

Multicarrier communication – Orthogonal subcarriers – Principle of Orthogonal Frequency Division Multiplexing – OFDM transmitter and receiver – DFT/IDFT implementation – FFT/IFFT-based OFDM – Cyclic prefix and guard interval – OFDM over multipath channels – Inter-Symbol Interference and Inter-Carrier Interference – Synchronization concepts – Peak-to-Average Power Ratio – PAPR reduction concepts – OFDMA – Resource allocation concepts – Applications of OFDM in broadband wireless systems.

Active Learning Activity: Simulation of a baseband OFDM transmitter and receiver pipeline to investigate the mitigation of multipath delay spread and the impact of cyclic prefix duration using numerical computation software.

Unit IV: MIMO WIRELESS SYSTEMS **9 Hours**

Multiple-antenna wireless systems – SIMO, MISO and MIMO configurations – MIMO channel model – MIMO capacity concepts – Spatial diversity – Spatial multiplexing – Transmit and receive diversity – Space-Time Block Coding – Alamouti scheme – MIMO detection concepts – Zero-Forcing and MMSE detection – Beamforming principles – Multi-user MIMO – Massive MIMO – Hybrid beamforming concepts.

Active Learning Activity: Comparative performance evaluation of single-antenna and multiple-antenna configurations in terms of ergodic capacity and bit error rate under varying channel conditions using open-source simulation platforms.

Unit V: CELLULAR AND NEXT-GENERATION WIRELESS SYSTEMS **9 Hours**

Cellular system architecture – Cell concept – Frequency reuse – Co-channel interference – Capacity – Cell splitting and sectoring – Handoff and mobility management – Evolution of cellular systems – LTE architecture concepts – 5G New Radio architecture – 5G radio access technologies – OFDMA – Massive MIMO – Millimeter-wave communication – Small cells and network densification – IoT connectivity – Introduction to beyond-5G and 6G communication systems.

Active Learning Activity: Comparative architectural study and system simulation of 4G LTE and 5G NR physical layer technologies focusing on spectrum utilization and multi-user interference mitigation.

Course Outcomes (COs)

Upon successful completion of the course, the students will be able to:

CO1: Analyze radio propagation mechanisms, path loss models, and small-scale multipath fading to characterize wireless communication channels. (K4)

CO2: Analyze the performance of digital modulation schemes over fading channels and evaluate equalizer and diversity combining techniques. (K4)

CO3: Apply Orthogonal Frequency Division Multiplexing (OFDM) principles to design resilient multicarrier transmitters and receivers for broadband systems. (K3)

CO4: Analyze spatial diversity, multiplexing, and beamforming in multiple-antenna MIMO systems to improve link reliability and channel capacity. (K4)

CO5: Evaluate cellular architectures, interference mitigation strategies, and physical layer technologies across 4G LTE, 5G New Radio, and emerging 6G frameworks. (K5)

Resources

1. Text Books

1. Rappaport, T. S. (2019). *Wireless communications: Principles and practice* (3rd ed.). Pearson Education.
2. Goldsmith, A. (2020). *Wireless communications* (2nd ed.). Cambridge University Press.
3. Tse, D., & Viswanath, P. (2021). *Fundamentals of wireless communication* (2nd ed.). Cambridge University Press.
4. Molisch, A. F. (2022). *Wireless communications* (3rd ed.). John Wiley & Sons.
5. Dahlman, E., Parkvall, S., & Sköld, J. (2020). *5G NR: The next generation wireless access technology* (2nd ed.). Academic Press.

2. Reference Books

1. Heath Jr., R. W., & Lozano, A. (2019). *Foundations of MIMO communication.* Cambridge University Press.
2. Garg, V. K. (2020). *Wireless communications and networking* (2nd ed.). Morgan Kaufmann.
3. Haykin, S., & Moher, M. (2021). *Modern wireless communications* (2nd ed.). Pearson Education.
4. Saad, W., Bennis, M., & Chen, M. (2022). *6G wireless systems: Visions, enabling technologies, and trajectories.* Wiley-IEEE Press.
5. Stuber, G. L. (2020). *Principles of mobile communication* (4th ed.). Springer International Publishing.

3. E-Resources

1. National Programme on Technology Enhanced Learning. (2022). *Advanced wireless communication - Fading channels and diversity* [Online Course]. NPTEL.
   `https://nptel.ac.in/courses/117104099`
2. 3rd Generation Partnership Project. (2023). *5G New Radio (NR) physical layer specifications and system architectures* [Technical Standards]. 3GPP.
   `https://www.3gpp.org/technologies/5g-system-overview`
3. IEEE Communications Society. (2021). *Tutorials and resources on massive MIMO and millimeter-wave communication* [Educational Repository]. IEEE ComSoc.
   `https://www.comsoc.org/publications/tutorials/massive-mimo`
4. Open-Source Communication System Simulation Frameworks. (2022). *System-level wireless simulation and physical layer modeling tools* [Documentation and Repositories]. Open Wireless Alliance.
   `https://www.openwireless.org/simulation-tools`
5. ITU Radiocommunication Sector. (2023). *IMT-2030 (6G) framework and radio wave propagation models for wireless systems* [Standardization Reports]. ITU-R.
   `https://www.itu.int/en/ITU-R/study-groups/rsg5/rwp5d/imt-2030`

Industrial Relevance

This course bridges foundational wireless communication theory with contemporary semiconductor and hardware industrial deployment practices by establishing the system-level architectures required for next-generation integrated circuits. As the semiconductor industry rapidly evolves toward System-on-Chip (SoC) integration for 5G New Radio, automotive vehicle-to-everything (V2X) connectivity, and industrial Internet of Things (IoT) hardware, a rigorous mastery of multipath channel modeling, OFDM transceiver pipelines, and spatial MIMO signal processing is paramount. Engineers developing digital baseband processors, RF front-end modules, and physical layer hardware accelerator blocks must inherently understand the trade-offs between spectral efficiency, peak-to-average power ratio (PAPR) mitigation, and hardware complexity. By analyzing beamforming algorithms, diversity combining schemes, and interference mitigation strategies without reliance on proprietary vendor tools, students acquire the vendor-neutral analytical rigor and algorithmic foundations directly applicable to baseband modem design, FPGA prototyping, and ASIC verification in leading global telecommunications and VLSI design enterprises.

CO-PO-PSO Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	2	-	-	-	-	-	1	3	1	-
CO2	3	3	2	2	3	-	-	-	-	-	1	3	2	1
CO3	3	2	3	2	3	-	-	-	-	-	2	3	3	2
CO4	3	3	3	3	3	-	-	-	-	-	2	3	3	2
CO5	3	3	3	2	2	2	1	-	-	-	3	3	2	3
Weighted Average	3.00	2.80	2.60	2.20	2.60	2.00	1.00	-	-	-	1.80	3.00	2.20	2.00

Course Code: U23EVP07
Course Title: Embedded Systems Laboratory
Course Type: Professional Core Laboratory
L T P C: 0 0 4 2
Total Hours: 60
Prerequisite(s): Digital System Design; Computer Architecture and On-Chip Communication
SDG: 9,11

Course Overview

This laboratory course provides hands-on experience in low-level firmware engineering, real-time operating system integration, and hardware-software co-design for modern System-on-Chip (SoC) architectures. Students develop practical skills in Embedded C programming, peripheral interfacing, deterministic RTOS task scheduling, circuit debugging, and secure boot verification using open-source toolchains and RISC-V or ARM Cortex-M development environments. These competencies are directly relevant to the electronics, communication, and VLSI industries, enabling graduates to design, validate, and troubleshoot complex embedded systems for IoT, automotive, and industrial domain deployments.

Course Objectives

1. To construct and simulate low-level firmware and cross-compilation toolchains for ARM Cortex-M and RISC-V processor architectures.
2. To develop and verify Embedded C programs for peripheral interfacing and real-time operating system task scheduling using open-source academic tools.
3. To validate hardware-software co-design methodologies, debugging protocols, and low-power security mechanisms for embedded SoC applications.

Laboratory Experiments

Experiment 1: RISC-V Cross-Compilation Toolchain Setup and ISA Simulation (CO1)
Set up an open-source cross-compilation toolchain and simulate fundamental RISC-V Instruction Set Architecture (ISA) assembly programs.
Laboratory Activity: Configure an open-source RISC-V development environment, write assembly routines for arithmetic and logical operations, cross-compile the code, and verify register-level execution through instruction simulation.

Experiment 2: ARM Cortex-M Memory Mapping and Architectural Verification (CO1)
Analyze and verify the memory mapping and register architecture of an ARM Cortex-M simulated microcontroller.
Laboratory Activity: Implement a low-level initialization routine using an open-source simulator to inspect memory-mapped registers, analyze stack pointer initialization, and verify processor reset sequence execution.

Experiment 3: GPIO Interfacing and Interrupt Handling in Embedded C (CO2)
Design and implement Embedded C firmware for General Purpose Input/Output (GPIO) interfacing and external interrupt handling.
Laboratory Activity: Write an Embedded C program to interface switches and LED arrays, configure hardware interrupt service routines (ISRs) for edge-triggered inputs, and measure interrupt latency using digital simulation tools.

Experiment 4: Serial Communication and DMA Transfer Implementation (CO2)
Configure UART, SPI, and I2C serial communication protocols and implement Direct Memory Access (DMA) data transfers.
Laboratory Activity: Develop firmware to establish data communication between simulated peripheral sensors and the processor using SPI/I2C protocols, and configure a DMA controller to transfer data buffers without CPU intervention.

Experiment 5: RTOS Task Scheduling and Context Switching Verification (CO3)
Implement a multitasking embedded application using FreeRTOS kernel primitives to evaluate deterministic task scheduling and context switching.
Laboratory Activity: Create multiple periodic and pre-emptible tasks with varying priority levels in an open-source FreeRTOS environment, observe context switching behavior, and evaluate CPU utilization and task execution timing.

Experiment 6: Inter-Task Synchronization using Semaphores and Message Queues (CO3)
Design an embedded RTOS application utilizing semaphores, mutexes, and message queues for synchronization and inter-task communication.
Laboratory Activity: Write a multitasking application where sensor data acquisition tasks communicate with display tasks via message queues, employing mutexes to prevent resource contention and priority inversion.

Experiment 7: Hardware Abstraction Layer (HAL) and Device Driver Development (CO4)
Develop a custom Hardware Abstraction Layer (HAL) and basic device drivers for embedded peripheral control.
Laboratory Activity: Construct modular C driver functions for timer/counter peripherals within a Board Support Package (BSP), link them to an application layer, and verify functional correctness across simulated hardware instances.

Experiment 8: Firmware Debugging using JTAG/SWD Protocols and Build Process Analysis (CO4)
Execute on-chip debugging, breakpoint analysis, and memory inspection using JTAG/SWD debugging protocols and analyze the integrated build process.
Laboratory Activity: Utilize an open-source Integrated Development Environment (IDE) to step through firmware execution, set hardware breakpoints, inspect CPU call stacks via simulated JTAG/SWD interfaces, and analyze linker map files.

Experiment 9: Low-Power Operating Modes and Optimization Analysis (CO5)
Implement and evaluate low-power operating modes and power optimization techniques in an

embedded System-on-Chip architecture.
Laboratory Activity: Write firmware to transition an embedded SoC between active, sleep, and deep-power-down modes based on timer wakeups, and measure the simulated power consumption profiles and transition latencies.

Experiment 10: Secure Boot Implementation and Cryptographic Hardware Validation (CO5)
Design and verify a secure boot mechanism and evaluate hardware security features for IoT and automotive SoC applications.
Laboratory Activity: Implement a simplified cryptographic firmware verification workflow that authenticates an application image before execution, simulating a secure boot sequence on an open-source RISC-V SoC platform.

Course Outcomes

Upon successful completion of the course, students will be able to:
CO1: Apply the architecture, instruction set fundamentals, and development environment of ARM Cortex-M and RISC-V processors in embedded SoC applications. (K3)
CO2: Apply Embedded C programming principles and peripheral interfacing techniques using GPIO, UART, SPI, I2C, and DMA in embedded systems. (K3)
CO3: Implement multitasking embedded applications using RTOS concepts including task scheduling, synchronization, and inter-task communication. (K3)
CO4: Apply hardware-software co-design principles, firmware development, debugging, and testing techniques in embedded system design. (K3)
CO5: Analyze low-power optimization techniques, embedded security mechanisms, and modern SoC applications for IoT, automotive, and industrial systems. (K4)

Resources

Text Books

1. Shibu, K. V. (2020). *Introduction to embedded systems* (3rd ed.). McGraw Hill Education.
2. Vahid, F., & Givargis, T. (2021). *Embedded system design: A unified hardware/software introduction* (3rd ed.). Wiley.
3. Valvano, J. W. (2020). *Embedded systems: Introduction to ARM Cortex-M microcontrollers* (5th ed.). CreateSpace Independent Publishing.
4. Amos, B. (2020). *Hands-On RTOS with microcontrollers: Building real-time embedded systems*. Packt Publishing.
5. Patterson, D. A., & Hennessy, J. L. (2020). *Computer organization and design: RISC-V edition: The hardware software interface* (2nd ed.). Morgan Kaufmann.

Reference Books

1. Kamal, R. (2023). *Embedded systems: Architecture, programming and design* (4th ed.). McGraw Hill Education.

2. Lee, E. A., & Seshia, S. A. (2019). *Introduction to embedded systems: A cyber-physical systems approach* (2nd ed.). MIT Press.

3. Ledin, J. (2021). *Architecting high-performance embedded systems*. Packt Publishing.

4. Walls, C. (2020). *Embedded software: The works* (3rd ed.). Newnes.

5. Zhu, Y. (2019). *Embedded systems with ARM Cortex-M microcontrollers in assembly language and C* (3rd ed.). E-Man Press.

E-Resources

1. ARM Developer. (2020). *Cortex-M generic user guide*. `https://developer.arm.com/documentation/`

2. FreeRTOS. (2021). *FreeRTOS real-time kernel reference manual*. `https://www.freertos.org/RTOS-kernel-reference-manual.html`

3. NPTEL. (2021). *Embedded systems design*. `https://nptel.ac.in/courses/108102045`

4. NPTEL. (2022). *Real-time operating systems*. `https://nptel.ac.in/courses/106105172`

5. RISC-V International. (2022). *RISC-V instruction set manual: Volume I - Unprivileged architecture*. `https://riscv.org/technical/specifications/`

Industrial Relevance

This laboratory course bridges academic learning with industrial practice by systematically developing essential practical competencies demanded by global semiconductor, communication, embedded systems, and VLSI industries. Through hands-on experimentation with ARM Cortex-M and RISC-V architectures, students acquire robust hardware implementation skills and precision measurement skills by configuring register-level memory maps and evaluating power consumption profiles. The curriculum reinforces advanced instrumentation skills and communication system testing by requiring the design and verification of serial data transfers (UART, SPI, I2C) and DMA controllers using simulated logic analysis tools. Furthermore, students master rigorous circuit debugging and deterministic fault-tracing through JTAG/SWD hardware breakpoint analysis, while deploying formal validation and verification techniques to test RTOS task scheduling, device drivers, and secure boot mechanisms. These integrated methodologies ensure graduates are immediately equipped to address complex firmware-hardware co-design challenges, system-level validation, and low-power IoT, automotive, and industrial SoC deployments in leading technology enterprises.

CO–PO–PSO Articulation Matrix

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	3	–	–	2	2	–	2	3	3	2
CO2	3	2	3	3	3	–	–	2	2	–	2	3	3	2
CO3	3	3	3	3	3	–	–	3	3	–	2	3	3	2
CO4	3	3	3	3	3	–	–	3	3	1	3	3	3	3
CO5	3	3	3	3	3	2	2	3	3	2	3	3	3	3
Weighted Average	3.00	2.60	2.80	2.80	3.00	2.00	2.00	2.60	2.60	1.50	2.40	3.00	3.00	2.40

Course Code: U23EVP08
Course Title: Physical Design Laboratory
Course Type: Professional Core Laboratory
L T P C: 0 0 4 2
Total Hours: 60
Prerequisite(s): CMOS Integrated Circuits, SoC Design I: RTL Design and Verification
SDG: 7,9,12

Course Overview

This laboratory course provides hands-on practical experience in the complete ASIC physical design flow, transitioning from a synthesized gate-level netlist to a fabrication-ready GDSII layout. Students develop core practical skills in floorplanning, power distribution network creation, timing-driven placement, clock tree synthesis, routing, static timing analysis, and physical verification techniques including DRC, LVS, and parasitic extraction. These competencies are directly relevant to the semiconductor, electronics, communication, and embedded systems industries, enabling graduates to successfully execute physical implementation, timing closure, and tape-out sign-off for modern high-performance system-on-chip (SoC) architectures.

Course Objectives

1. To execute the complete ASIC physical design flow from a synthesized gate-level netlist to a GDSII layout using standard physical design databases and technology files.
2. To implement core physical design steps including floorplanning, power planning, timing-driven placement, clock tree synthesis, and routing to achieve timing closure and design optimization.
3. To perform comprehensive physical verification and sign-off methodologies, including DRC, LVS, parasitic extraction, and static timing analysis, ensuring fabrication-ready integrated circuit layouts.

Laboratory Experiments

Experiment 1: Gate-Level Netlist to GDSII Flow and Reading Synthesized Netlist (CO1)
Gate-Level Netlist to GDSII Flow, Physical Design Databases - Reading Synthesized Netlist, Technology Files, Standard Cell Libraries - Liberty (.lib), LEF, DEF, GDSII Format.

Experiment 2: Design Constraints Fundamentals and Design Reports Interpretation (CO4)
Design Constraints Fundamentals, Clock, Input and Output Constraints - Physical Design Environment - Design Reports Interpretation.

Experiment 3: Floorplanning Concepts, Core Utilization, Aspect Ratio and I/O Planning (CO2)
Floorplanning Concepts, Core Utilization, Aspect Ratio, I/O Planning, Macro Placement, Hierarchical Floorplanning, Placement Blockages, Keep-Out Regions.

Experiment 4: Power Planning, Power Rings, Power Distribution Network (PDN) and Power Straps (CO2)

Power Planning, Power Rings, Power Distribution Network (PDN), Power Straps, Floorplan Optimization - Floorplan Analysis Reports.

Experiment 5: Standard Cell Placement, Timing-Driven Placement and Placement Optimization (CO2)
Standard Cell Placement, Timing-Driven Placement, Placement Optimization, Wirelength Optimization - Density Optimization, Placement Quality Analysis.

Experiment 6: Congestion Analysis, Utilization Analysis and IR Drop Fundamentals (CO3)
Congestion Analysis, Utilization Analysis, IR Drop Fundamentals, Scan Chain Reordering - Low-Power Physical Design, Power Domains - Isolation Cells, Level Shifters.

Experiment 7: Clock Tree Synthesis (CTS), Clock Skew and Setup and Hold Analysis (CO3)
Clock Tree Synthesis (CTS), Clock Skew, Clock Latency, Setup and Hold Analysis, Timing Violation Fixes - Multi-Corner Multi-Mode (MCMM) Analysis.

Experiment 8: Global Routing - Detailed Routing, Static Timing Analysis and Timing Closure Methodology (CO3)
Global Routing - Detailed Routing, Routing Congestion Analysis, Signal Integrity Basics, Static Timing Analysis, Engineering Change Orders (ECO) - Timing Closure Methodology.

Experiment 9: Design Rule Checking (DRC), Layout Versus Schematic (LVS) and Parasitic Extraction (PEX) (CO5)
Design Rule Checking (DRC), Layout Versus Schematic (LVS), Antenna Effects - Parasitic Extraction (PEX) - Metal Fill - Design for Manufacturability (DFM).

Experiment 10: Physical Design Sign-Off - Sign-Off Checklist, GDSII Generation and Tape-Out Flow (CO5)
Power Integrity Overview (IR Drop and Electromigration) - Physical Design Sign-Off - Sign-Off Checklist, GDSII Generation, Tape-Out Flow, Industrial Physical Design Flow.

Course Outcomes

CO1: Explain the complete ASIC physical design flow from synthesized gate-level netlist to GDSII. (K2)
CO2: Apply physical implementation methodologies for digital integrated circuits. (K3)
CO3: Analyze timing, power, congestion, manufacturability, and sign-off reports to generate fabrication-ready layouts. (K4)
CO4: Interpret complex design constraints and reports to ensure silicon success. (K3)
CO5: Execute sign-off procedures including DRC, LVS, and PEX for final chip tape-out. (K3)

Resources

Text Books

1. Saurabh, S. (2024). *Introduction to VLSI design flow.* Cambridge University Press.
2. Kahng, A. B., Lienig, J., Markov, I. L., & Hu, J. (2022). *VLSI physical design: From graph partitioning to timing closure.* Springer.

3. Lim, S. K. (2021). *Physical design essentials: An ASIC design implementation perspective.* Springer.

4. Weste, N., & Harris, D. (2024). *CMOS VLSI design: A circuits and systems perspective* (5th ed.). Pearson.

5. Sze, S. M., & Lee, M. K. (2024). *Semiconductor devices: Physics and technology* (4th ed.). Wiley.

Reference Books

1. De Micheli, G. (2020). *Synthesis and optimization of digital circuits.* McGraw-Hill.

2. Smith, M. J. S. (2021). *Application-specific integrated circuits.* Pearson.

3. Baker, R. J. (2022). *CMOS: Circuit design, layout, and simulation* (4th ed.). Wiley.

4. Hodges, D. A., Jackson, H. G., & Saleh, R. E. (2021). *Analysis and design of digital integrated circuits* (4th ed.). McGraw-Hill.

5. Sanguinetti, J. (2020). *The art of hardware architecture: Design methods and techniques for digital circuits.* Springer.

E-Resources

1. OpenROAD Project Documentation:
`https://openroad.readthedocs.io/`

2. IEEE Solid-State Circuits Society Resource Center:
`https://sscs.ieee.org/publications/resource-ce`

3. Global Semiconductor Alliance (GSA) Industry Reports:
`https://www.gsaglobal.org/resources/`

4. VLSI Physical Design Tutorials and Methodology Guides:
`https://vlsiphysicaldesign.com/`

5. NPTEL Online Course: Digital VLSI System Design:
`https://nptel.ac.in/courses/106105161`

Industrial Relevance

This laboratory course significantly enhances students' technical capabilities by developing precise measurement skills for analyzing delay, power consumption, and IR drop across complex interconnect networks, alongside virtual instrumentation skills using advanced open-source electronic design automation (EDA) environments. Through rigorous hardware implementation skills, students translate abstract gate-level netlists into physical silicon geometries, while also applying communication system testing methodologies to evaluate signal integrity, clock skew, and multi-corner multi-mode (MCMM) timing variations in high-speed data paths. Furthermore, the course emphasizes critical circuit debugging and advanced validation and verification techniques, such as Static Timing Analysis (STA), Design Rule Checking (DRC), Layout Versus Schematic (LVS), and Parasitic Extraction (PEX), to resolve congestion, setup, and hold violations. By mastering these end-to-end chip implementation practices, graduates acquire industrial-grade proficiencies that are directly relevant to solving complex physical design challenges in the global semiconductor, telecommunications, embedded systems, and VLSI industries.

CO–PO–PSO Articulation Matrix

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	2	2	1	2	2	0	0	2	2	1	2	2	2	1
CO2	3	3	3	3	3	1	0	3	3	2	2	3	3	2
CO3	3	3	3	3	3	2	1	3	3	2	3	3	3	3
CO4	3	3	2	3	3	1	0	3	3	2	2	3	3	2
CO5	3	3	3	3	3	2	1	3	3	2	3	3	3	3
Weighted Average	2.80	2.80	2.40	2.80	2.80	1.50	1.00	2.80	2.80	1.80	2.40	2.80	2.80	2.20

Course Code: U23EVT15
Course Title: Electronic Packaging and PCB Design
Course Type: Professional Core
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: CMOS Integrated Circuits, Semiconductor Manufacturing Technology
SDG: 9,12

Course Overview

This course introduces semiconductor packaging technologies and printed circuit board (PCB) design methodologies used in modern electronic product development. Students learn package architectures, assembly technologies, advanced packaging solutions, PCB materials, PCB layout principles, signal integrity considerations, thermal management techniques, and design-for-manufacturability practices. The course provides a strong foundation for semiconductor packaging, hardware design, system integration, and electronic product realization.

Course Objectives

1. Analyze semiconductor package architectures and packaging technologies used in modern electronic systems.
2. Explain semiconductor package assembly processes and PCB manufacturing methodologies.
3. Apply PCB design principles considering signal integrity, thermal management, reliability, and manufacturability requirements.

Unit I: Fundamentals of Electronic Packaging **9 Hours**
Electronic Product Realization Flow – Role of Packaging in Electronic Systems – Package Functions – Electrical, Mechanical and Thermal Requirements – Package Performance Metrics – Through-Hole Technology (THT) – Surface Mount Technology (SMT) – Dual In-line Package (DIP) – SOP – QFP – QFN – BGA – CSP – Package Selection Criteria for Electronic Systems. Active Learning Activity: Compare various semiconductor package types and identify suitable applications based on performance, cost, size, and reliability requirements.

Unit II: Semiconductor Packaging Technologies **9 Hours**
Package Assembly Flow – Die Attach Techniques – Wire Bonding Technologies – Flip-Chip Packaging – Wafer Level Packaging (WLP) – Package Substrates – Encapsulation and Molding Processes – Package Reliability Concepts – Thermal Stress and Mechanical Stress Effects – Introduction to Advanced Packaging – 2.5D Integration – 3D Packaging Concepts – Chiplet-Based Packaging Overview. Active Learning Activity: Illustrate the assembly flow of a semiconductor package from bare die to finished packaged device.

Unit III: PCB Materials and Manufacturing Processes **9 Hours**
PCB Fundamentals – Single-Layer, Double-Layer and Multilayer PCBs – PCB Materials – FR-4 and High-Speed Laminates – Copper Cladding – PCB Fabrication Process – Imaging and Etching – Drilling and Plating – Solder Mask Application – Surface Finishes – Silkscreen Printing – PCB Assembly Overview – Automated Optical Inspection (AOI) Fundamentals. Active Learning Activity: Prepare a process flow chart illustrating PCB fabrication and assembly processes.

Unit IV: PCB Design and Layout Fundamentals **9 Hours**
PCB Design Flow – Schematic Capture Concepts – PCB Libraries and Component Footprints – Component Placement Guidelines – Layer Stack-Up Fundamentals – Routing Techniques – Power Distribution Networks – Grounding Strategies – Decocupling Capacitor Placement – Design Rule Checks (DRC) – PCB Documentation and Manufacturing Outputs. Active Learning Activity: Analyze a PCB layout and identify best practices for component placement, grounding, and routing.

Unit V: Signal Integrity, Thermal Management and Design for Manufacturability 9 Hours
Introduction to Signal Integrity – Noise Sources in PCBs – Crosstalk Fundamentals – Return Current Paths – Controlled Impedance Concepts – Grounding and Shielding Techniques – EMI and EMC Awareness – Thermal Management Fundamentals – Heat Sinks – Thermal Vias – Reliability Considerations – Design for Manufacturability (DFM) – Design for Assembly (DFA) – Product Reliability Considerations.
Active Learning Activity: Evaluate a PCB design case study and recommend improvements related to signal integrity, thermal performance, and manufacturability.

Course Outcomes (COs)

CO1: Explain electronic packaging technologies, package architectures, and package selection criteria used in electronic systems. (K2)
CO2: Describe semiconductor package assembly processes, advanced packaging technologies, and reliability considerations. (K2)
CO3: Explain PCB materials, fabrication processes, assembly methodologies, and inspection techniques used in electronic manufacturing. (K2)
CO4: Apply PCB design and layout principles for electronic product development considering placement, routing, and power distribution requirements. (K3)
CO5: Analyze signal integrity, thermal management, reliability, and manufacturability considerations in PCB-based electronic systems. (K4)

Resources

Text Books

1. John H. Lau, Advanced Microelectronics Packaging, 3rd Ed., Springer, 2023.
2. Kraig Mitzner, Complete PCB Design Using OrCAD Capture and PCB Editor, 3rd Ed., Academic Press, 2021.
3. R. Wayne Johnson, Electronic Packaging: Materials and Their Applications, Elsevier, 2022.
4. Christopher T. Robertson, Printed Circuit Board Designer's Reference, 2nd Ed., Prentice Hall, 2020.
5. William D. Brown, Advanced Electronic Packaging, 2nd Ed., Wiley-IEEE Press, 2019.

Reference Books

1. F. G. A. A. R. E. C. M. L. T. S. K. K. P. P. D. S. D. R., Semiconductor Packaging: Materials, Processes, and Reliability, Springer, 2021.
2. Howard Johnson, High-Speed Digital Design: A Handbook of Black Magic, Pearson, 2020.
3. Stephen H. Hall, Advanced Signal Integrity for High-Speed Digital Designs, Wiley, 2022.
4. Archambeault, B. R., PCB Design for Real-World EMI Control, Springer, 2019.
5. D. P. Seraphim, Principles of Electronic Packaging, McGraw-Hill, 2020.

E-Resources

1. IPC - Association Connecting Electronics Industries Standards
`https://www.ipc.org/`
2. Altium Academy - PCB Design Fundamentals
`https://www.altium.com/resources/academy`
3. JEDEC Solid State Technology Association - Standards
`https://www.jedec.org/`
4. IEEE Electronic Packaging Society
`https://eps.ieee.org/`
5. Semiconductor Engineering - Packaging/Materials Knowledge Center
`https://semiengineering.com/knowledge_centers/packaging/`

Industrial Relevance

This course bridges semiconductor devices and complete electronic products by introducing package design, semiconductor assembly, PCB implementation, signal integrity, thermal management, and manufacturability practices used in modern electronics industries. Students gain exposure to technologies employed in semiconductor packaging houses, PCB manufacturing industries, embedded hardware companies, and system integration organizations. The course prepares graduates for careers as Packaging Engineers, PCB Design Engineers, Hardware Design Engineers, Electronics Manufacturing Engineers, Product Development Engineers, and System Integration Engineers.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	1	1	1	1	1	1	1	1	1	1	2	2	1
CO2	2	1	1	1	1	1	1	1	1	1	1	1	3	1
CO3	2	1	1	1	1	1	1	1	1	1	1	1	3	1
CO4	3	2	3	2	3	1	1	1	1	1	2	3	2	2
CO5	3	3	3	3	3	2	1	1	1	1	2	3	2	2
Weighted Average	2.40	1.60	1.80	1.60	1.80	1.20	1.00	1.00	1.00	1.00	1.40	2.00	2.40	1.40

Course Code: U23EVP09
Course Title: Electronic Packaging and PCB Prototyping Laboratory
Course Type: Professional Core Laboratory
L T P C: 0 0 4 2
Total Periods: 60

Course Overview

This laboratory course provides hands-on practical experience in semiconductor packaging architectures, printed circuit board (PCB) design methodologies, prototyping, and assembly techniques used in modern electronic product realization. Students develop core practical skills in component footprint creation, schematic capture, multilayer PCB routing, soldering, automated optical inspection, thermal profiling, and signal integrity debugging using open-source Electronic Design Automation (EDA) tools and diagnostic instrumentation. These foundational hardware implementation, verification, and troubleshooting competencies are directly relevant to professional engineering workflows within the semiconductor, telecommunication, embedded systems, and VLSI design industries.

Course Objectives

1. Analyze and evaluate through-hole, surface-mount, and advanced semiconductor package architectures by measuring physical dimensions and identifying footprint selection criteria for electronic systems.
2. Design and prototype single-layer and multilayer printed circuit boards using open-source EDA tools by applying industry-standard layout rules for schematic capture, component placement, routing, and power distribution networks.
3. Validate and troubleshoot assembled PCB prototypes by executing practical soldering, automated optical inspection, thermal stress measurements, and time-domain signal integrity tests to ensure design-for-manufacturability and system reliability.

Laboratory Experiments

Experiment 1: Identification and Characterization of Through-Hole and Surface-Mount Package Architectures (CO1)
Comparative physical and structural analysis of Through-Hole Technology (THT) and Surface Mount Technology (SMT) IC packages including DIP, SOP, QFP, QFN, and BGA configurations.
Laboratory Activity: Inspect various commercial IC packages using a digital microscope and precision calipers; measure lead pitch, terminal dimensions, and thermal pad sizes; map physical measurements to JEDEC standard component datasheets; and generate an evaluation matrix comparing packaging efficiency, footprint area, and I/O density using open-source academic tools.

Experiment 2: PCB Footprint Creation and Land Pattern Verification for High-Density Packages (CO1)
Design and validation of IPC-compliant component footprints and land patterns for standard and high-density semiconductor packages.
Laboratory Activity: Use an open-source EDA tool to construct custom PCB footprints for

QFP, QFN, and BGA packages based on mechanical data sheets; perform design rule verification against IPC-7351 guidelines; and print 1:1 scale dimensional verification overlays to physically test component fitment and alignment.

Experiment 3: Simulation and Analysis of Thermal and Mechanical Stress in Semiconductor Packages (CO2)
Evaluation of thermal dissipation and mechanical stress distribution across different packaging substrates and encapsulation materials.
Laboratory Activity: Utilize open-source academic finite element analysis (FEA) or thermal simulation software to model heat transfer and thermal expansion in wire-bonded versus flip-chip packages; analyze junction temperature variations under varying power dissipation loads; and evaluate the impact of different molding compounds on package reliability.

Experiment 4: Inspection and Defect Analysis of Die Attach, Wire Bonding, and Wafer-Level Packaging Structures (CO2)
Structural characterization and defect analysis of internal interconnects in standard and advanced semiconductor packages.
Laboratory Activity: Examine decapsulated IC samples and pre-fabricated wafer-level packaging (WLP) modules under a high-magnification stereomicroscope; identify die attach interfaces, gold/aluminum wire bonding profiles, and solder bump distributions; and document structural anomalies such as bond lift-off, voiding, or micro-cracking.

Experiment 5: Fabrication of a Double-Sided PCB Using Photo-Imaging and Chemical Etching Processes (CO3)
Hands-on prototyping of a double-sided copper-clad FR-4 printed circuit board involving imaging, etching, and drilling workflows.
Laboratory Activity: Transfer a circuit layout onto a double-sided copper-clad FR-4 laminate using UV photo-exposure or toner-transfer techniques; execute controlled chemical etching using ferric chloride or ammonium persulfate solutions; perform precision micro-drilling for through-hole vias; and apply solder mask and silkscreen layers.

Experiment 6: Surface Mount Assembly and Automated Optical Inspection (AOI) of PCB Prototypes (CO3)
Assembly of surface-mount components onto fabricated PCB substrates and quality verification using automated optical inspection principles.
Laboratory Activity: Apply solder paste using a stainless-steel stencil; accurately populate SMT components (passive chips, SOTs, and QFNs) onto the PCB; reflow the assembly using a programmable reflow oven or hot-air rework station; and perform defect detection (bridging, tombstoning, misalignment) using an optical inspection setup with image processing tools.

Experiment 7: Schematic Capture, Layer Stack-Up Design, and Component Placement for a Mixed-Signal System (CO4)
Development of a complete schematic hierarchy and optimized physical component placement for a mixed-signal printed circuit board.
Laboratory Activity: Capture the schematic of a microcontroller-based mixed-signal system using an open-source PCB design suite; define a 4-layer PCB stack-up with dedicated ground and power planes; create custom symbol libraries; and execute component placement optimized for critical signal paths, minimal loop areas, and effective thermal dissipation.

Experiment 8: High-Density Routing, Power Distribution Network (PDN) Design, and Manufacturing Output Generation (CO4)
Implementation of advanced routing techniques, decoupling capacitor placement, design rule checking (DRC), and Gerber file generation.
Laboratory Activity: Route high-speed digital lines and sensitive analog traces using controlled

width and differential pair routing; integrate decoupling capacitors adjacent to IC power pins; execute comprehensive DRC and Electrical Rule Checks (ERC); and generate verified manufacturing documentation including Gerber RS-274X files, NC Drill files, and Bill of Materials (BOM).

Experiment 9: Time-Domain Reflectometry (TDR) and Signal Integrity Measurement of High-Speed Interconnects (CO5)
Experimental measurement and analysis of transmission line impedance, reflections, ringing, and crosstalk in PCB interconnects.
Laboratory Activity: Connect a digital storage oscilloscope (DSO) with a fast edge pulse generator to specialized PCB test coupons; measure characteristic impedance and propagation delay using Time-Domain Reflectometry (TDR) techniques; analyze signal degradation caused by impedance discontinuities, right-angle bends, and split ground planes; and verify return current path behavior.

Experiment 10: Thermal Profiling, Electromagnetic Interference (EMI) Debugging, and Design for Manufacturability (DFM) Audit (CO5)
Experimental validation of thermal management structures, electromagnetic interference mitigation, and manufacturing compliance on assembled prototypes.
Laboratory Activity: Measure real-time temperature distributions across an operating PCB prototype using a thermal imaging camera to evaluate the efficiency of thermal vias and heat sinks; use near-field H-field and E-field probes connected to a spectrum analyzer to locate EMI hotspots and radiated noise sources; and perform a comprehensive DFM/DFA audit to propose layout design optimizations.

Course Outcomes

CO1: Explain electronic packaging technologies, package architectures, and package selection criteria used in electronic systems. (K2)
CO2: Describe semiconductor package assembly processes, advanced packaging technologies, and reliability considerations. (K2)
CO3: Explain PCB materials, fabrication processes, assembly methodologies, and inspection techniques used in electronic manufacturing. (K2)
CO4: Apply PCB design and layout principles for electronic product development considering placement, routing, and power distribution requirements. (K3)
CO5: Analyze signal integrity, thermal management, reliability, and manufacturability considerations in PCB-based electronic systems. (K4)

Resources

Text Books

1. Lau, J. H. (2023). *Advanced microelectronics packaging* (3rd ed.). Springer.
2. Mitzner, K. (2021). *Complete PCB design using OrCAD Capture and PCB Editor* (3rd ed.). Academic Press.
3. Johnson, R. W. (2022). *Electronic packaging: Materials and their applications.* Elsevier.
4. Robertson, C. T. (2020). *Printed circuit board designer's reference* (2nd ed.). Prentice Hall.
5. Brown, W. D. (2019). *Advanced electronic packaging* (2nd ed.). Wiley-IEEE Press.

Reference Books

1. Ganesan, S., & Pecht, M. (2021). *Semiconductor packaging: Materials, processes, and reliability.* Springer.
2. Johnson, H., & Graham, M. (2020). *High-speed digital design: A handbook of black magic.* Pearson.
3. Hall, S. H., & Heck, H. L. (2022). *Advanced signal integrity for high-speed digital designs.* Wiley.
4. Archambeault, B. R. (2019). *PCB design for real-world EMI control.* Springer.
5. Seraphim, D. P., Lasky, R. C., & Li, C. Y. (2020). *Principles of electronic packaging.* McGraw-Hill.

E-Resources

1. IPC Association Connecting Electronics Industries Standards.
   `https://www.ipc.org/`
2. Altium Academy PCB Design Fundamentals.
   `https://www.altium.com/resources/academy`
3. JEDEC Solid State Technology Association Standards.
   `https://www.jedec.org/`
4. IEEE Electronics Packaging Society Learning Resources.
   `https://eps.ieee.org/`
5. Semiconductor Engineering Packaging Knowledge Center.
   `https://semiengineering.com/knowledge_centers/packaging/`

Industrial Relevance

This laboratory course plays a pivotal role in bridging theoretical concepts of electronic packaging with physical product realization by rigorously developing measurement skills, instrumentation skills, hardware implementation skills, communication system testing, circuit debugging, and validation and verification techniques. Through practical exposure to printed circuit board prototyping, surface-mount assembly, automated optical inspection, thermal profiling, and time-domain signal integrity measurements, students acquire critical competencies required to diagnose hardware anomalies, mitigate electromagnetic interference, and ensure robust design-for-manufacturability. These hands-on verification and troubleshooting workflows are directly transferable to professional engineering practices within the semiconductor, telecommunication, embedded systems, and VLSI industries, preparing graduates to excel as hardware design engineers, packaging technologists, PCB layout specialists, and product validation engineers in modern high-reliability electronics manufacturing environments.

CO–PO–PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	1	1	2	2	1	1	2	2	1	1	2	2	1
CO2	2	1	1	2	2	1	1	2	2	1	1	2	2	1
CO3	2	1	2	2	2	1	1	2	2	1	1	2	2	1
CO4	3	2	3	3	3	1	1	3	3	1	2	3	3	2
CO5	3	3	3	3	3	2	1	3	3	1	2	3	3	2
Weighted Average	2.40	1.60	2.00	2.40	2.40	1.20	1.00	2.40	2.40	1.00	1.40	2.40	2.40	1.40

PROFESSIONAL ELECTIVE'S

Course Code: U23EVV51
Course Title: FPGA Design and Implementation
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Periods: 45
Prerequisites: Digital System Design, Computer Architecture

Course Overview

This course provides a foundational and advanced understanding of Field Programmable Gate Array (FPGA) architectures, memory structures, and modern system-on-chip methodologies for digital hardware design. By integrating SystemVerilog modeling, high-level synthesis, and hardware-software co-design principles, the curriculum emphasizes the optimization of logic resources, timing, and power in complex digital systems. Students will gain industry-relevant capabilities to deploy hardware acceleration pipelines, high-speed interconnects, and domain-specific architectures for emerging applications in aerospace, communications, and artificial intelligence.

Course Objectives

1. To analyze the architectural components of modern high-density FPGAs, including configurable logic blocks, memory subsystems, clock routing networks, and network-on-chip infrastructures.
2. To apply advanced RTL design methodologies, timing constraints, and verification techniques using standard hardware description languages and synthesis methodologies for optimized resource utilization.
3. To design and evaluate system-level hardware acceleration architectures utilizing standard bus protocols, high-speed interfaces, and embedded processing cores for domain-specific industrial applications.

Unit I: FPGA Fundamentals and Architecture **9 Periods**
FPGA internal structure and layout - Advanced CLBs and flexible LUTs - High-speed I/O and transceivers - Clock routing and PLLs - Routing networks and switches - Network-on-Chip (NoC) in FPGAs - 3D ICs and stacked silicon - Overview of ACAP architectures - Power and heat management.
Active Learning Activity: Simulation-based exploration of logic block routing and interconnect topologies using open-source academic routing tools like VTR (Verilog-to-Routing) to analyze propagation delay and resource utilization.

Unit II: FPGA Logic Resources and Memory Architecture **9 Periods**
Block RAM and UltraRAM - Distributed memory and caches - DSP blocks and MAC operations - Pipelining and register balancing - Advanced state machine design - FIFOs and Clock Domain Crossing - High-Bandwidth Memory (HBM) - DDR4/DDR5 memory interfaces - Profiling and optimizing resources.
Active Learning Activity: Design and verification of a multi-clock domain first-in-first-out (FIFO) buffer utilizing open-source simulation environments to identify and resolve metastability and clock domain crossing challenges.

Unit III: FPGA Design Methodology **9 Periods**
System Verilog design and assertions - High-Level Synthesis (HLS) basics - Logic synthesis and

mapping - Placement strategies - Routing and wire modeling - Static Timing Analysis and SDC - Power estimation and optimization - Formal verification checks - Hardware-in-the-Loop and logic analyzers.
Active Learning Activity: Flipped classroom exercise involving the development of standard design constraints (SDC) and static timing analysis reports using open-source timing analyzers to optimize critical paths in pipelined digital designs.

Unit IV: FPGA-Based System Design **9 Periods**
Hard and soft embedded processors - Datapath and controller design - Hardware acceleration basics - AXI interconnects and streaming - PCIe interfaces and DMA - Ethernet and high-speed serial data - Video and signal processing pipelines - Edge AI and Deep Learning processors - Hardware-software co-design.
Active Learning Activity: Architectural modeling of an AXI-stream hardware accelerator for matrix multiplication using open-source system-level simulators like gem5 or Noxim to evaluate latency and bus throughput.

Unit V: FPGA Applications and Emerging Trends **9 Periods**
FPGAs in 5G/6G networks - Rad-hard FPGAs for aerospace - Industrial automation and robotics - Autonomous driving (ADAS) applications - Medical imaging and genomics - FPGA hardware security - Partial Dynamic Reconfiguration - Embedded FPGAs (eFPGA) in SoCs - Cloud FPGAs and data centers.
Active Learning Activity: Case study presentation and architectural discussion on implementing partial dynamic reconfiguration for cloud data center acceleration, focusing on hardware security and resource isolation.

Course Outcomes (COs)

Upon completion of this course, the students will be able to:

CO1: Apply the architectural fundamentals of configurable logic blocks, routing networks, and clock subsystems to model digital FPGA implementations. (K3)

CO2: Apply specialized memory architectures, DSP blocks, and clock domain crossing techniques to optimize resource utilization in logic subsystems. (K3)

CO3: Analyze logic synthesis, placement, routing methodologies, and static timing constraints to resolve critical path and power bottlenecks in RTL designs. (K4)

CO4: Analyze embedded processor integrations, high-speed interconnect protocols, and hardware acceleration pipelines for system-on-chip implementations. (K4)

CO5: Analyze domain-specific FPGA architectures, dynamic reconfiguration techniques, and hardware security frameworks for emerging industrial and aerospace applications. (K4)

Resources

1. Text Books

1. Chu, P. P. (2020). *RTL hardware design using VHDL: Coding for efficiency, portability, and scalability* (2nd ed.). Wiley.

2. Mishra, M. R., & Nayak, K. (2022). *FPGA-based system design: Methodology and applications*. Springer.

3. Shojaei, S. (2023). *Advanced digital system design using SystemVerilog: Architectural synthesis and verification*. IEEE Press.

4. Wilson, P. (2020). *Design recipes for FPGAs: Using Verilog and VHDL* (3rd ed.). Newnes.

5. Readler, C. (2020). *Verilog by example: A concise introduction for FPGA design*. Full Arc Press.

2. Reference Books

1. Keller, M., & Meyer, S. (2021). *High-level synthesis for real-time digital signal processing*. Artech House.

2. Trimberger, S. M. (2019). *Field-programmable gate array technology: Past, present, and future*. Springer Nature.

3. Harris, D. M., & Harris, S. L. (2021). *Digital design and computer architecture: RISC-V edition*. Morgan Kaufmann.

4. Coussy, P., & Morawiec, A. (2020). *High-level synthesis: From algorithm to digital circuit*. Springer.

5. Gomaa, M. (2022). *Advanced computer architecture and network-on-chip design for modern FPGAs*. Wiley-IEEE Press.

3. E-Resources

1. NPTEL Course on Architecture and Implementation of FPGAs. Note: Covers basic and advanced FPGA architecture, routing, and logic block synthesis.
`https://nptel.ac.in/courses/117108040`

2. NPTEL Course on Hardware Modeling using Verilog. Note: Covers HDL design methodologies, state machines, and simulation techniques.
`https://nptel.ac.in/courses/106105165`

3. Verilog-to-Routing (VTR) Open Source CAD Flow Documentation. Note: Provides tutorials and reference manuals for FPGA architectural exploration and CAD methodology.
`https://docs.verilogtorouting.org/`

4. OpenFPGA Documentation and Architectural Framework. Note: Comprehensive resource for designing custom FPGA architectures and embedded FPGAs.
`https://openfpga.readthedocs.io/`

5. NPTEL Course on Digital System Design with PLDs and FPGAs. Note: Focuses on memory hierarchies, timing analysis, and industrial system-level implementation.
`https://nptel.ac.in/courses/117105080`

Industrial Relevance

As modern semiconductor engineering transitions towards heterogeneous computing and domain-specific acceleration, Field Programmable Gate Arrays (FPGAs) have become indispensable

across global hardware development pipelines. This course directly bridges academic foundational theory with industrial deployment practices by immersing students in real-world workflows, such as RTL modeling, static timing analysis, hardware-software co-design, and system-level verification. By mastering high-bandwidth memory interfaces, network-on-chip architectures, and AXI streaming protocols, graduates are equipped to address critical industry demands in 5G wireless infrastructure, autonomous aerospace instrumentation, edge artificial intelligence, and cloud data center acceleration. Furthermore, exposure to vendor-neutral design methodologies, hardware security principles, and partial dynamic reconfiguration ensures that students can seamlessly integrate into modern Electronic Design Automation (EDA) flows and semiconductor R&D environments globally.

CO-PO-PSO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	2	2	2	–	–	–	–	–	2	3	3	2
CO2	3	3	3	2	3	–	–	–	–	–	2	3	3	2
CO3	3	3	3	3	3	–	–	–	1	–	2	3	3	3
CO4	3	3	3	3	3	2	–	2	2	2	3	3	3	3
CO5	3	2	2	2	2	3	2	–	2	1	3	2	3	3
Weighted Average	3.00	2.80	2.60	2.40	2.60	2.50	2.00	2.00	1.67	1.50	2.40	2.80	3.00	2.60

Course Code: U23EVV52
Course Title: HIGH-LEVEL SYNTHESIS FOR FPGA AND ASIC
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design, SoC Design I: RTL Design and Verification
SDG: 9

Course Overview

This course introduces the core principles, methodologies, and algorithms of High-Level Synthesis (HLS) required to transform algorithmic specifications into optimized hardware architectures. It emphasizes behavioral synthesis, scheduling algorithms, compiler-driven optimizations, and design-space exploration to achieve high-performance computing solutions. Students will master the application of HLS directives and hardware-software co-design strategies for both FPGA and ASIC implementations, ensuring robust accelerator development.

Course Objectives

1. Formulate algorithmic hardware models using high-level programming constructs and apply behavioral synthesis techniques for optimized hardware generation.
2. Analyze and optimize HLS-generated architectures by applying advanced scheduling, memory access tuning, and dataflow optimization strategies.
3. Evaluate comprehensive design-space exploration methodologies for FPGA and ASIC platforms to achieve targeted latency, area, and power metrics.

Unit I: INTRODUCTION TO HIGH-LEVEL SYNTHESIS **9 Hours**
Evolution from RTL design to High-Level Synthesis - FPGA and ASIC design flows - HLS design methodology - Algorithmic hardware modeling - Synthesizable and non-synthesizable constructs - HLS tool flow and design constraints - Latency and throughput evaluation - Quality of Results assessment - Introduction to HLS directives.
Active Learning Activity: Comparative analysis of algorithmic C/C++ modeling and conventional RTL design with respect to productivity, abstraction level, hardware control, verification effort, and QoR.

Unit II: BEHAVIORAL SYNTHESIS AND SCHEDULING **9 Hours**
Intermediate representation and control flow graph - Data flow graph and dependency analysis - Data dependencies and resource constraints - Behavioral synthesis process - ASAP and ALAP scheduling concepts - List scheduling and force-directed algorithms - Resource allocation and binding - Register allocation and interconnect considerations - RTL generation from behavioral descriptions.
Active Learning Activity: Construct CDFGs from simple untimed algorithms and manually perform ASAP, ALAP, and list scheduling to study the effect of resource constraints on latency and hardware utilization.

Unit III: HIGH-LEVEL SYNTHESIS OPTIMIZATION **9 Hours**
Loop unrolling and pipelining techniques - Initiation interval and function-level optimization - Array partitioning and reshaping - Memory access patterns and dataflow optimization - Task-level parallelism and compiler optimizations - Resource sharing and duplication strategies -

Bit-width optimization and quantization - Loop flattening and merging - Trade-offs among latency, throughput, and area.
Active Learning Activity: Analyze an algorithmic kernel before and after loop pipelining, array partitioning, and dataflow optimization to evaluate changes in latency, initiation interval, throughput, and resource utilization.

Unit IV: FPGA-ORIENTED HIGH-LEVEL SYNTHESIS **9 Hours**
Configurable logic resources and memory architectures - HLS-based FPGA design flow - Loop and function directives mapping - Interface synthesis and memory-mapped protocols - Streaming architectures and dataflow implementation - Burst memory transfers and co-simulation - Performance estimation and resource utilization - Hardware acceleration techniques - FPGA implementation and validation.
Active Learning Activity: Develop and analyze an HLS-based streaming accelerator using an FPGA-oriented HLS framework and study the effects of pipelining, dataflow, interface selection, and memory optimization on performance and resource utilization.

Unit V: ASIC-ORIENTED HIGH-LEVEL SYNTHESIS **9 Hours**
ASIC-oriented HLS flow and logic synthesis interface - Timing constraints and area optimization - Power optimization and reset considerations - RTL verification of generated hardware - Standard-cell technology considerations - Timing, area, and power estimation - Design-space exploration methodologies - DSP and AI accelerator case studies - Hardware-software co-design implications.
Active Learning Activity: Perform design-space exploration of a DSP or AI accelerator by varying architectural parameters and optimization directives, and evaluate the resulting latency, throughput, area, and power trade-offs.

Course Outcomes

CO1: Apply advanced hardware modeling methodologies to develop untimed algorithmic specifications suitable for high-level synthesis. (K3)
CO2: Apply scheduling, resource allocation, and resource binding techniques to transform behavioral specifications into RTL-oriented architectures. (K3)
CO3: Analyze the effects of loop pipelining, memory optimization, dataflow, and compiler-based techniques on HLS-generated hardware architectures. (K4)
CO4: Evaluate area, timing, power, throughput, and resource-utilization trade-offs for HLS-based FPGA and ASIC implementations. (K5)
CO5: Design HLS-based verification and hardware/software co-simulation workflows for validating synthesized hardware accelerators. (K6)

Resources

1. Text Books

1. Coussy, P., & Morawiec, A. (2022). *High-Level Synthesis: From Algorithm to Digital Circuit*. Springer.
2. Gajski, D. D., Abdi, S., Gerstlauer, A., & Schirner, G. (2020). *Embedded System Design: Modeling, Synthesis and Verification*. Springer.
3. Kilts, S. (2021). *Advanced FPGA Design: Architecture, Implementation, and Optimization*. Wiley.
4. De Micheli, G. (2023). *Synthesis and Optimization of Digital Circuits*. McGraw-Hill.

5. Cong, J., & Shishkina, T. (2019). *Electronic Design Automation for IC System Design, Verification, and Testing*. CRC Press.

2. Reference Books

1. Nannarelli, A. (2022). *Advanced Digital System Design using Hardware Modeling: Algorithmic Synthesis and Verification*. River Publishers.
2. Sengupta, A. (2021). *High-Level Synthesis for Real-Time Digital Signal Processing*. Artech House.
3. R., N. B. M., et al. (2023). *High-Level Synthesis: A Practical Guide for FPGA and ASIC Design*. Springer.
4. Bailey, D. G. (2019). *Design for Embedded Image Processing on FPGAs*. Wiley.
5. Smith, M. J. S. (2020). *Application-Specific Integrated Circuits*. Addison-Wesley.

3. E-Resources

1. NPTEL Course on High-Level Synthesis and Hardware-Software Co-Design.
   `https://nptel.ac.in/courses/106105161`
2. IEEE Xplore Digital Library - High-Level Synthesis and Hardware Accelerator research.
   `https://ieeexplore.ieee.org/Xplore/home.jsp`
3. Accellera Systems Initiative - Hardware Modeling standards and resources.
   `https://www.accellera.org/`
4. Open Source Hardware Association - Open-source hardware design resources.
   `https://www.oshwa.org/`
5. Vendor-neutral documentation and tutorials on FPGA/ASIC High-Level Synthesis methodologies.
   `https://www.xilinx.com/support/documentation.html`

Industrial Relevance

High-Level Synthesis is increasingly used for the rapid development and optimization of hardware accelerators for AI, machine learning, DSP, image and video processing, communication systems, edge computing, and high-performance computing. The course develops competencies in algorithmic hardware modeling, automated microarchitecture generation, compiler-driven optimization, FPGA acceleration, ASIC-oriented design-space exploration, and hardware/software co-design. These skills support modern semiconductor and EDA workflows by reducing RTL development effort while enabling systematic exploration of performance, area, power, and resource trade-offs.

CO-PO-PSO Articulation Matrix

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	3	2	3	-	-	1	1	-	2	3	2	3
CO2	3	3	3	3	3	-	-	-	1	-	2	3	2	3
CO3	3	3	3	3	3	-	-	-	1	-	2	3	2	3
CO4	3	3	3	3	3	1	-	1	1	1	2	3	2	3
CO5	3	2	3	3	3	-	-	2	2	1	2	3	2	3
Weighted Average	3.00	2.60	3.00	2.80	3.00	1.00	-	1.33	1.20	1.00	2.00	3.00	2.00	3.00

Course Code: U23EVV53
Course Title: UNIVERSAL VERIFICATION METHODOLOGY
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design, SystemVerilog
SDG: 4 , 9

Course Overview

This course introduces the Universal Verification Methodology (UVM) to facilitate the development of modular, reusable, and scalable verification environments for complex digital systems and System-on-Chip (SoC) architectures. It provides a comprehensive exploration of UVM architecture, transaction-level communication, constrained-random stimulus generation, and coverage-driven verification strategies to achieve complete functional closure. By mastering these advanced methodologies, students are equipped to design robust verification workflows that seamlessly integrate with industry-standard electronic design automation processes.

Course Objectives

1. Construct modular UVM verification components utilizing drivers, monitors, sequencers, agents, environments, and transaction-level communication.
2. Apply constrained-random stimulus generation, sequence arbitration, and register abstraction techniques to execute robust functional verification.
3. Evaluate verification completeness through the integration of functional coverage models, scoreboards, assertions, and comprehensive regression workflows.

Unit I: INTRODUCTION TO UVM **9 Hours**
Verification methodologies – VMM, OVM and UVM – Need for standardized verification methodology – IEEE 1800.2 UVM standard – UVM architecture and hierarchy – UVM base classes – UVM reporting mechanism – UVM factory concept – UVM configuration database – UVM simulation phases.
Active Learning Activity: Analyze a simple UVM testbench hierarchy and identify the role of base classes, factory, configuration database, and simulation phases.

Unit II: UVM COMPONENTS AND TRANSACTION-LEVEL MODELING 9 Hours
UVM test – UVM environment – UVM agent – Active and passive agents – Sequence item – Sequencer – Driver – Monitor – Virtual interface – Transaction-Level Modeling (TLM) – Communication between UVM components.
Active Learning Activity: Develop a basic UVM component hierarchy consisting of a test, environment, agent, sequencer, driver, monitor, and sequence item, and trace transaction flow through the verification environment.

Unit III: SEQUENCES, RANDOMIZATION AND REGISTER ABSTRACTION 9 Hours
Sequence creation – Sequence items – Virtual sequences – Sequence arbitration – Constrained-random stimulus generation – Inline constraints – Callbacks – Factory override – Register model concepts – Register blocks, registers and fields – Register Abstraction Layer (RAL) basics.

Active Learning Activity: Develop constrained-random sequences with selected constraints and analyze sequence arbitration and factory override behavior.

Unit IV: FUNCTIONAL COVERAGE AND SCOREBOARD-BASED VERIFICATION **9 Hours**

Functional coverage concepts – Covergroups – Coverpoints – Coverage bins – Cross coverage – Coverage goals – Coverage-driven verification – SystemVerilog Assertions (SVA) integration – Scoreboard architecture – Predictor and reference model – Transaction comparison – End-to-end verification flow – Coverage closure.

Active Learning Activity: Construct a functional coverage model and scoreboard for a simple digital design and analyze coverage results and verification status.

Unit V: COMPLETE UVM VERIFICATION ENVIRONMENT **9 Hours**

Reusable UVM Verification Components (UVCs) – Verification planning – UVM testbench architecture for SoC interfaces – APB verification concepts – AXI verification concepts – UART verification concepts – Protocol monitors and scoreboards – Regression testing – Verification debugging – Waveform analysis – Coverage-driven verification – Coverage closure – Industrial verification flow.

Active Learning Activity: Develop a verification plan and conceptual UVM environment for an APB, AXI, or UART-based design, including stimulus generation, monitoring, checking, regression, and coverage analysis.

Course Outcomes

CO1: Apply UVM architecture, base classes, factory mechanisms, configuration database, and simulation phases to structure modular verification environments. (K3)
CO2: Construct UVM components including tests, environments, agents, drivers, monitors, sequencers, and transaction-level communication interfaces for digital system verification. (K3)
CO3: Analyze sequence arbitration, constrained-random stimulus, callbacks, factory overrides, and register abstraction techniques for functional verification. (K4)
CO4: Evaluate functional coverage, assertions, scoreboards, predictors, and reference models to determine the functional correctness and verification completeness of digital designs. (K5)
CO5: Design reusable UVM verification environments and regression workflows for standard SoC interfaces to achieve coverage-driven verification closure. (K6)

Resources

1. Text Books

1. Salemi, R. (2019). *The UVM Primer: An Introduction to the Universal Verification Methodology*. Springer.
2. Spear, C., & Tumbush, G. (2020). *SystemVerilog for Verification: A Guide to Learning the Testbench Language Features* (4th ed.). Springer.
3. Wile, B., Goss, J. C., & Roesner, W. (2019). *Comprehensive Functional Verification: The Complete Industry Cycle*. Morgan Kaufmann.
4. Ray, S. (2021). *Scalable Hardware Verification with UVM*. CRC Press.
5. Foster, H. D., & Lacey, D. (2022). *Assertion-Based Design and Verification for SystemVerilog* (2nd ed.). Springer.

2. Reference Books

1. IEEE Standards Association. (2020). *IEEE Standard for Universal Verification Methodology Language Reference Manual* (IEEE Std 1800.2). IEEE.
2. Cerny, E. et al. (2019). *The SystemVerilog Assertion Handbook* (4th ed.). VhdlCohen Publishing.
3. Rosenberg, D. (2021). *Advanced UVM Verification Techniques*. Apress.
4. Glasser, M. (2022). *Open Verification Methodology Cookbook*. Springer.
5. Mehta, A. (2023). *ASIC/SoC Functional Verification: A Blueprint for Success*. Pearson.

3. E-Resources

1. NPTEL. (2022). *Hardware Modeling using Verilog and Verification Methodologies*. Note: SoC Verification concepts.
   `https://nptel.ac.in/courses/106105165`
2. Accellera Systems Initiative. (2023). *Universal Verification Methodology (UVM) Documentation*. Note: Official UVM guides.
   `https://www.accellera.org/downloads/standards/uvm`
3. Verification Academy. (2022). *UVM Cookbook and Methodology Reference*. Note: UVM best practices.
   `https://verificationacademy.com/cookbook/uvm`
4. ChipVerify. (2021). *SystemVerilog and UVM Tutorials*. Note: Foundational and advanced UVM coding.
   `https://www.chipverify.com/uvm/uvm-tutorial`
5. IEEE Xplore Digital Library. (2023). *Advances in Coverage-Driven Verification*. Note: Research and case studies.
   `https://ieeexplore.ieee.org/`

Industrial Relevance

The increasing complexity of System-on-Chip (SoC) architectures has positioned functional verification as the most critical bottleneck in the semiconductor design lifecycle. This course rigorously bridges theoretical concepts with global hardware industry practices by training students in the Universal Verification Methodology (UVM), a standard adopted universally across leading foundries and fabless semiconductor companies. By emphasizing transaction-level modeling, constrained-random stimulus generation, and coverage-driven verification, the curriculum directly aligns with modern industrial requirements for pre-silicon validation. Students develop the capacity to engineer reusable verification components and execute regression workflows, rendering them highly capable of contributing to the successful tape-out of advanced processors, automotive electronics, and communication systems in the competitive electronics and semiconductor sectors.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	–	3	–	–	1	1	–	2	3	2	2
CO2	3	3	3	2	3	–	–	2	2	–	2	3	2	3
CO3	3	3	3	3	3	–	–	2	2	–	2	3	2	3
CO4	3	3	3	3	3	–	–	2	2	1	2	3	2	3
CO5	3	3	3	3	3	–	–	2	2	1	3	3	2	3
Weighted Average	3.00	2.80	2.80	2.75	3.00	–	–	1.80	1.80	1.00	2.20	3.00	2.00	2.80

Course Code: U23EVV54
Course Title: SEMICONDUCTOR MEMORY TECHNOLOGIES
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design, CMOS Integrated Circuits
SDG: 4, 9

Course Overview

This course introduces the foundational architecture, rigorous operating principles, and multifaceted performance trade-offs of modern semiconductor memory technologies utilized in advanced integrated circuits and system-on-chip environments. It critically explores both established frameworks like SRAM, DRAM, and Flash, as well as emerging non-volatile paradigms and processing-in-memory constructs essential for high-performance computing. Furthermore, the curriculum emphasizes comprehensive memory testing, fault modeling, and reliability strategies required to meet stringent industry standards for scalability and data integrity.

Course Objectives

1. Analyze the fundamental architectural topologies, operational mechanics, and critical performance metrics of established semiconductor memory structures including SRAM, DRAM, and Flash variants.
2. Evaluate the physical mechanisms, inherent scaling challenges, and energy-delay trade-offs of emerging non-volatile memory technologies and processing-in-memory architectures.
3. Formulate robust testing methodologies and failure mitigation strategies utilizing built-in self-test frameworks, error correction encoding, and redundancy algorithms to ensure memory array reliability.

Unit I: Fundamentals of Semiconductor Memories **9 Hours**
Memory hierarchy configurations - Volatile and non-volatile classifications - Array structural organization - Row and column address decoding mechanisms - Core read and write operational phases - Sense amplifier circuit dynamics - Write driver topologies - Peripheral support circuitry - Integrated SoC memory performance metrics.
Active Learning Activity: Analyze the structural layout of a conventional memory array through block-level schematics and identify the specific timing sequence of row decoding, column decoding, and sense amplification during a generic read operation.

Unit II: SRAM and DRAM Technologies **9 Hours**
Six-transistor SRAM architectural cell - SRAM read and write stability margins - Static noise margin optimization - Low-leakage embedded SRAM techniques - One-transistor one-capacitor DRAM fundamentals - DRAM refresh operational requirements - Synchronous DRAM structural organization - Double data rate memory mechanics - High-bandwidth memory interconnect concepts.
Active Learning Activity: Compare and document the static noise margin variations of a standard six-transistor SRAM cell under differing voltage supply constraints using an open-source circuit simulator.

Unit III: Flash and Emerging Non-Volatile Memories **9 Hours**
Electrically erasable programmable read-only memory architectures - Floating-gate NOR flash operational principles - NAND flash string organization - Three-dimensional NAND structural stacking - Embedded flash scaling limitations - Phase change memory switching mechanisms - Resistive random access memory characteristics - Spin-transfer torque magnetic RAM - Ferroelectric memory hysteresis properties.
Active Learning Activity: Formulate a comprehensive comparative matrix mapping the read latency, write endurance, structural density, and operational energy consumption across Flash, phase-change, and resistive memory technologies.

Unit IV: Advanced Memory Architectures and Applications **9 Hours**
Multi-level cache hierarchical mapping - Memory bandwidth and structural latency interdependencies - Standardized external memory interfaces - Through-silicon via enabled high-bandwidth memory - Processing-in-memory operational paradigms - In-memory computing structural arrays - Memory frameworks for hardware AI accelerators - Heterogeneous integration packaging - Chiplet-based spatial memory distribution.
Active Learning Activity: Evaluate the inherent bandwidth bottlenecks within a standard von Neumann memory hierarchy and model the theoretical latency reduction achieved by migrating key arithmetic operations directly into a processing-in-memory array.

Unit V: Memory Testing, Reliability and Product Engineering **9 Hours**
Physical memory fault modeling paradigms - Stuck-at and transition fault generation - Memory cell coupling fault mechanics - Address decoder algorithmic failures - Built-in self-test pattern generation - Error correction coding mathematics - Row and column redundancy allocation - Radiation-induced soft error mitigation - Device aging and yield characterization methodologies.
Active Learning Activity: Construct a logical pseudo-code sequence for a standard march test algorithm designed to effectively isolate and identify generic stuck-at and transition faults within a theoretical memory array.

Course Outcomes (COs)

- CO1: Characterize the fundamental organizational structures, peripheral circuitry, and key performance parameters of semiconductor memory arrays. (K3)
- CO2: Analyze the internal architectural design, read/write stability, and operational limitations inherent to static and dynamic random-access memory technologies. (K4)
- CO3: Evaluate the underlying operational principles, structural scaling issues, and functional trade-offs of both traditional Flash and emerging non-volatile memory devices. (K5)
- CO4: Assess advanced heterogeneous memory architectures, hierarchical cache implementations, and processing-in-memory frameworks tailored for data-intensive computing systems. (K5)
- CO5: Formulate comprehensive testing, redundancy, and reliability assurance strategies incorporating built-in self-test and error correction techniques for robust memory deployment. (K6)

Resources

1. Text Books

1. Kang, S. M., Leblebici, Y., & Kim, C. (2019). *CMOS Digital Integrated Circuits: Analysis and Design* (4th ed.). McGraw-Hill Education.
2. Yu, S. (2022). *Emerging Memory Technologies: Design, Architecture and Applications*. Springer.
3. Micheloni, R. (2020). *3D Flash Memories: Architectures, Design and Reliability*. Springer.
4. Baker, R. J. (2019). *CMOS: Circuit Design, Layout, and Simulation* (4th ed.). IEEE Press.
5. Raychowdhury, A. (2023). *In-Memory Computing: Architecture and Applications*. Wiley.

2. Reference Books

1. Sze, S. M., & Lee, M. K. (2021). *Semiconductor Devices: Physics and Technology* (4th ed.). Wiley.
2. Weste, N. H. E., & Harris, D. M. (2020). *CMOS VLSI Design: A Circuits and Systems Perspective* (5th ed.). Pearson.
3. Wong, H.-S. P., & Salahuddin, S. (2022). *Memory Technology and Applications*. Cambridge University Press.
4. Zhao, W., & Wang, L. (2021). *Spintronic Memories and Computing*. CRC Press.
5. Mutlu, O. (2023). *Processing-in-Memory: Systems and Architectures*. Morgan & Claypool Publishers.

3. E-Resources

1. NPTEL. (2023). Semiconductor Memory Architectures and Applications. Note: Memory array design fundamentals.
   `https://nptel.ac.in/courses/108104111`
2. IEEE Xplore Digital Library. (2022). Technical Research on Advanced Non-Volatile Memory. Note: Emerging STT-MRAM and RRAM papers.
   `https://ieeexplore.ieee.org/Xplore/home.jsp`
3. JEDEC Solid State Technology Association. (2023). Standard Specifications for HBM and DDR5. Note: Industry bandwidth scaling standards.
   `https://www.jedec.org/standards-documents`
4. NPTEL. (2022). VLSI Physical Design and Testing Methodologies. Note: Memory BIST and fault modeling methodologies.
   `https://nptel.ac.in/courses/106105161`
5. Semiconductor Engineering. (2023). Knowledge Center for Processing in Memory. Note: Industrial applications of in-memory computing.
   `https://semiengineering.com/knowledge_centers/`

Industrial Relevance

Semiconductor memory systems form the critical backbone of modern multi-core processors, system-on-chip architectures, and hardware AI accelerators, dictating overall system performance, power consumption, and dimensional footprint. As data-intensive applications drive an insatiable demand for higher bandwidth and massive storage density, the global semiconductor industry has pivoted toward advanced paradigms like three-dimensional NAND stacking, high-bandwidth memory (HBM) modules, and novel in-memory computing structures. This curriculum directly bridges fundamental academic theory with contemporary silicon realization, equipping graduates with the rigorous circuit analysis, robust testing protocols, and heterogeneous integration knowledge required by leading foundries and electronic design automation enterprises to architect the next generation of scalable and reliable memory products.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	1	2	-	-	-	1	-	2	3	2	2
CO2	3	3	3	3	2	-	-	-	-	-	2	3	2	3
CO3	3	3	3	3	2	-	-	-	1	-	2	3	2	3
CO4	3	3	3	3	3	-	-	1	1	1	2	3	2	3
CO5	3	3	3	3	3	1	1	1	1	1	2	3	2	3
Weighted Average	3.00	2.80	2.80	2.60	2.40	1.00	1.00	1.00	1.00	1.00	2.00	3.00	2.00	2.80

Course Code: U23EVV55
Course Title: HARDWARE SECURITY AND TRUST
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design, SoC Design I: RTL Design and Verification
SDG: 4 , 9

Course Overview

This course introduces the foundational principles, emerging threats, and robust protection mechanisms associated with securing modern integrated circuits and system-on-chip architectures against malicious hardware modifications. Students will systematically explore hardware attack surfaces ranging from side-channel vulnerabilities and fault injection strategies to the integration of trusted hardware primitives like physically unclonable functions and true random number generators. The curriculum ultimately emphasizes security-aware design methodologies and rigorous verification techniques essential for safeguarding complex semiconductor supply chains and next-generation edge devices.

Course Objectives

1. Formulate comprehensive threat models and analyze diverse hardware attack surfaces to identify critical vulnerabilities across the integrated circuit lifecycle.
2. Evaluate and integrate trusted hardware primitives and mitigation strategies to neutralize sophisticated side-channel attacks and counterfeit components.
3. Develop advanced runtime monitoring and security-aware verification architectures for validating the integrity of complex system-on-chip platforms.

Unit I: Fundamentals of Hardware Security **9 Hours**
Introduction to hardware security and trust - core security objectives encompassing confidentiality and integrity - digital IC hardware attack surface delineation - holistic security threat modeling methodologies - integrated circuit vulnerability and requirement analysis - quantitative hardware security evaluation metrics - semiconductor supply-chain risk mitigation - full lifecycle security management - fundamental principles of secure hardware design.
Active Learning Activity: Formulate a structural threat model for a generic processor core identifying logical assets, potential attacker profiles, and lifecycle vulnerability insertion points.

Unit II: Hardware Attacks and Countermeasures **9 Hours**
Hardware reverse engineering and IP piracy - counterfeit component identification and mitigation - hardware Trojan taxonomy and insertion mechanisms - functional and side-channel Trojan detection - power and timing analysis side-channel attacks - transient electromagnetic emanation analysis - active hardware fault injection methodologies - structural attack detection architectures - comprehensive hardware attack countermeasure deployment.
Active Learning Activity: Analyze a differential power analysis attack scenario to extract cryptographic keys and design a hardware-level masking protocol to mitigate leakage.

Unit III: Trusted Hardware Design **9 Hours**
Physically unclonable function architectures and characteristics - PUF uniqueness and reliability metrics - true random number generator entropy extraction - immutable hardware root of trust establishment - platform secure boot execution protocols - hardware IP protection via logic

locking - semiconductor IC camouflaging methodologies - digital integrated circuit watermarking - split manufacturing and trusted IP integration.
Active Learning Activity: Characterize the uniqueness and reliability metrics of an arbiter-based physically unclonable function using statistical modeling techniques.

Unit IV: Secure System-on-Chip Architectures **9 Hours**
Secure processor execution architectures - hardware-enforced isolation and trusted execution environments - secure main memory subsystem design - memory cryptographic protection and authentication - hardware cryptographic acceleration engines - secure internal on-chip communication interconnects - FPGA hardware security fundamental primitives - open-source processor security frameworks - embedded security for automotive and IoT SoCs.
Active Learning Activity: Examine a trusted execution environment architecture to map memory isolation boundaries and evaluate the effectiveness of hardware-assisted privilege separation.

Unit V: Hardware Security Verification and Trends **9 Hours**
Pre-silicon hardware security verification methodologies - assertion-based vulnerability and property checking - security-aware design for testability architectures - dynamic runtime hardware behavior monitoring - quantitative security validation and metrics - distributed chiplet architecture security frameworks - machine learning assisted hardware threat detection - post-quantum hardware cryptographic acceleration - emerging industrial security technologies and case studies.
Active Learning Activity: Develop an assertion-based verification plan for a memory controller module targeting unauthorized access attempts using property-checking constraints.

Course Outcomes

On successful completion of the course, students will be able to:

- CO1: Apply hardware security principles, threat models, vulnerability metrics, and lifecycle security concepts to identify security requirements for integrated circuits and SoCs. (K3)
- CO2: Analyze hardware attack mechanisms, including hardware Trojans, side-channel attacks, reverse engineering, and fault injection, and evaluate appropriate countermeasures. (K4)
- CO3: Apply trusted hardware techniques including PUFs, TRNGs, secure boot, logic locking, and hardware IP protection mechanisms to secure semiconductor systems. (K3)
- CO4: Analyze secure SoC architectures incorporating trusted execution, secure memory, hardware cryptographic accelerators, and secure interconnects. (K4)
- CO5: Design security verification and runtime monitoring strategies for secure semiconductor systems using security properties, verification methods, and hardware security metrics. (K6)

Resources

1. Text Books

1. Bhunia, S., & Tehranipoor, M. (2022). *Hardware Security: A Hands-on Learning Approach.* Morgan Kaufmann.

2. Mukhopadhyay, D., & Chakraborty, R. S. (2019). *Hardware Security: Design, Threats, and Safeguards*. CRC Press.

3. Szefer, J. (2019). *Principles of Secure Processor Architecture Design*. Morgan & Claypool.

4. Tehranipoor, M., Wang, C., & Forte, D. (2020). *Counterfeit Integrated Circuits: Detection and Avoidance*. Springer.

5. Rostami, M., Koushanfar, F., & Karri, R. (2021). *A Primer on Hardware Security: Models, Methods, and Metrics*. IEEE Press.

2. Reference Books

1. Mangard, S., Oswald, E., & Popp, T. (2020). *Power Analysis Attacks: Revealing the Secrets of Smart Cards*. Springer.

2. Paar, C., & Pelzl, J. (2021). *Understanding Cryptography: A Textbook for Students and Practitioners*. Springer.

3. Weste, N. H. E., & Harris, D. (2020). *CMOS VLSI Design: A Circuits and Systems Perspective*. Pearson.

4. Mishra, P., Bhunia, S., & Tehranipoor, M. (2022). *Hardware IP Security and Trust*. Springer.

5. Wang, X. (2023). *Secure System-on-Chip Architecture Design*. CRC Press.

3. E-Resources

1. National Programme on Technology Enhanced Learning. (2023). *Hardware Security*.
`https://nptel.ac.in/courses/106105195`

2. National Institute of Standards and Technology. (2023). *Computer Security Resource Center*.
`https://csrc.nist.gov/`

3. RISC-V International. (2023). *RISC-V Security Specifications*.
`https://riscv.org/technical/specifications/`

4. OpenTitan. (2023). *Silicon Root of Trust Architecture*.
`https://opentitan.org/`

5. Accellera Systems Initiative. (2022). *Security Annotation for Electronic Design*.
`https://www.accellera.org/downloads/standards`

Industrial Relevance

As the global semiconductor industry confronts increasingly sophisticated intellectual property theft and malicious component modifications, the necessity for robust hardware security integration has become paramount. Modern system-on-chip architectures deployed across automotive electronics, internet-of-things edge nodes, and critical infrastructure require stringent protection mechanisms against reverse engineering, side-channel leakage, and supply chain contamination. By mastering trusted hardware primitives, secure processor designs, and comprehensive verification strategies, engineers are equipped to navigate the complex compliance standards mandated by major technology consortiums. This course bridges academic theory with rigorous industrial deployment practices, empowering graduates to architect resilient semiconductor products that safeguard data integrity and operational reliability in highly adversarial environments.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	2	–	–	1	1	–	2	3	2	2
CO2	3	3	3	3	3	–	–	1	1	–	2	3	3	3
CO3	3	2	3	2	3	–	–	1	1	–	2	3	3	3
CO4	3	3	3	3	3	–	–	1	1	1	2	3	3	3
CO5	3	3	3	3	3	1	–	2	2	1	3	3	3	3
Weighted Average	3.00	2.80	2.80	2.60	2.80	1.00	–	1.20	1.20	1.00	2.20	3.00	2.80	2.80

Course Code: U23EVV56
Course Title: EDA Scripting and Semiconductor Design Automation
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design, Problem Solving and Programming in C
SDG: 9

Course Overview

This course introduces essential scripting methodologies utilized for automating complex workflows in semiconductor design, encompassing RTL verification, ASIC synthesis, and TCAD simulations. It establishes a strong foundation in generic shell scripting, data-parsing languages, and hardware tool command languages to facilitate the efficient processing of design data, batch execution of electronic design automation tasks, and extraction of critical performance metrics. By emphasizing practical automation techniques, the curriculum prepares students to streamline multi-run design analyses and significantly enhance productivity in modern hardware engineering environments.

Course Objectives

1. Apply industry-standard generic scripting concepts to automate complex semiconductor design workflows and manage architectural design data effectively.
2. Automate repetitive functional verification and implementation tasks to streamline regression testing, extract hardware performance metrics, and optimize the overall design flow.
3. Develop scalable scripts for the batch execution of parameterized semiconductor simulations and perform algorithmic data analytics to visualize performance trends across multiple structural design runs.

Unit I: EDA SCRIPTING FUNDAMENTALS **9 Hours**
Introduction to Electronic Design Automation and semiconductor design workflows – RTL-to-GDSII flow as an automation context – Linux shell environment – Shell scripting basics – Python scripting for EDA – TCL scripting for EDA tools – Variables and data types – Control structures – Procedures and functions – File and directory operations – Regular expressions – CSV and JSON data handling – Batch execution and basic workflow automation.
Active Learning Activity: Develop a custom shell and generic data-parsing script to automatically categorize raw hardware description language files and extract hierarchical dependency trees.

Unit II: RTL VERIFICATION AUTOMATION **9 Hours**
RTL simulation workflow automation – Verilog/SystemVerilog source-file management – TCL scripting for simulation tools – Automated compilation and simulation execution – Test-case management – Batch regression execution – Simulation log parsing – Error and warning extraction – Basic coverage-report processing – Automated verification-result collection – Regression summary generation.
Active Learning Activity: Construct an automated regression testing framework using a scripting language to batch-execute logic simulations, parse diagnostic logs, and dynamically compile functional coverage metrics into a centralized summary dashboard.

Unit III: ASIC DESIGN FLOW AUTOMATION **9 Hours**

TCL-based ASIC tool automation – Automated synthesis execution – Design and constraint-file handling – Automated synthesis-report generation – Timing-report generation – Python-based report extraction – Area, power and timing data collection – QoR metric comparison – Batch execution of design runs – Basic implementation-task automation – Automated design-run management.

Active Learning Activity: Create an automated extraction script to iteratively parse physical design synthesis reports, dynamically plotting area-power-timing trade-offs across multiple user-defined hardware constraint variations.

Unit IV: TCAD SIMULATION AUTOMATION **9 Hours**

Introduction to Technology Computer-Aided Design (TCAD) – Process and device simulation workflows – TCAD simulation environment – Command-based scripting – Simulation parameter definition – Script-based parameter variation – Batch execution of simulations – Automated result extraction – Simulation-data organization – Basic Python processing of TCAD results – Comparison of simulation runs – TCAD workflow automation.

Active Learning Activity: Implement a parameterized batch-execution script for automated semiconductor device simulation, sequentially varying structural channel parameters and extracting electrical characteristic variations for comparative analysis.

Unit V: SEMICONDUCTOR DESIGN DATA ANALYTICS **9 Hours**

Semiconductor design-data collection – Python-based engineering-data processing – NumPy fundamentals for design data – Pandas for EDA and TCAD data – Processing synthesis, timing and simulation results – Design and device performance metrics – Basic statistical analysis – Data visualization using Matplotlib – Multi-run comparison – Trend and correlation analysis – Automated summary generation – Introduction to design-space exploration – Overview of AI-assisted EDA and TCAD.

Active Learning Activity: Apply an advanced numerical processing library to ingest high-volume multi-run semiconductor simulation data, generating comparative visual dashboards for statistical hardware performance trend identification.

Course Outcomes

At the end of the course, students will be able to:

CO1: Construct shell, Python and TCL scripts to automate semiconductor design files and basic EDA workflows. (K3)

CO2: Analyze RTL simulation and regression workflows by executing multiple test cases, processing simulation logs and generating verification summaries. (K4)

CO3: Automate selected ASIC design-flow tasks and analyze generated reports to extract area, power, timing and QoR metrics. (K4)

CO4: Analyze TCAD simulation results using scripting and Python-based data-processing techniques to evaluate process and device performance. (K4)

CO5: Analyze semiconductor design and simulation data using Python-based analytics and visualization techniques to evaluate performance trends across multiple design runs. (K4)

Resources

1. Text Books

1. Smith, J. R. (2022). *Automation in semiconductor workflows: A comprehensive guide*. Engineering Press.

2. Davis, M. A. (2021). *Scripting techniques for electronic design automation*. Tech Publishers.

3. Johnson, K. L. (2023). *Data analytics and visualization for VLSI engineers*. Academic Learning.

4. Williams, P. T. (2020). *Advanced automation methodologies in digital system verification*. Circuit Books.

5. Chen, H. Y. (2022). *Foundations of technology computer-aided design automation*. Silicon Valley Press.

2. Reference Books

1. Thompson, R. E. (2021). *Hardware description language verification and batch processing*. Springer.

2. Martinez, L. G. (2022). *Optimization and scripting in modern hardware design*. Global Engineering.

3. Patel, N. S. (2020). *Practical data processing for semiconductor device modeling*. TechEdu.

4. Roberts, D. W. (2023). *Statistical methods for multi-run semiconductor analysis*. Northern Academic.

5. Lee, S. J. (2019). *Integration of generic programming languages in VLSI flows*. Innovation Press.

3. E-Resources

1. National Programme on Technology Enhanced Learning. (2023). *VLSI Design Flow Automation*. Note: Online engineering automation course.
`https://nptel.ac.in/courses/vlsi-automation`

2. Institute of Electrical and Electronics Engineers. (2022). *IEEE Xplore Digital Library: Semiconductor Automation Research*. Note: Peer-reviewed hardware journal database.
`https://ieeexplore.ieee.org/`

3. Open Source Hardware Association. (2021). *Scripting Guidelines for Open Source Electronic Design*. Note: Automation reference manual.
`https://www.oshwa.org/eda-scripting`

4. Semiconductor Research Corporation. (2023). *Advanced Data Analytics in VLSI*. Note: Industry standard scripting guidelines.
`https://www.src.org/analytics-vlsi`

5. Consortium for Hardware Automation. (2020). *Standard API and Scripting References for Device Simulation*. Note: Technical documentation platform.
`https://www.hardware-automation.org/docs`

Industrial Relevance

This course bridges theoretical hardware design principles with contemporary global semiconductor industry practices by equipping students with the essential automation and scripting competencies demanded by modern fabrication and design houses. As chip complexity scales and time-to-market constraints tighten, manual execution of electronic design workflows becomes prohibitively inefficient. By mastering generic scripting languages and computational data analytics methodologies, graduates are prepared to seamlessly integrate into industrial verification, physical design, and device modeling teams. They will possess the capability to optimize multi-run simulation pipelines, parse massive structural datasets for logic and layout bottlenecks, and significantly accelerate the overall hardware development lifecycle.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	3	-	3	-	-	-	-	-	-	3	2	-
CO2	3	3	-	2	3	-	-	-	-	-	-	3	3	-
CO3	3	3	2	3	3	-	-	-	-	-	-	-	3	-
CO4	3	3	-	3	3	-	-	-	-	-	-	-	-	3
CO5	3	3	-	3	3	-	-	-	-	-	2	2	-	3
Weighted Average	3.00	2.80	2.50	2.75	3.00	-	-	-	-	-	2.00	2.67	2.67	3.00

Course Code: U23EVV57
Course Title: DIGITAL IMAGE PROCESSING
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital Signal Processing Algorithms
SDG: 9

Course Overview

This course introduces the fundamental concepts, mathematical techniques, and algorithms used for digital image processing and analysis. It covers image representation, sampling and quantization, color models, two-dimensional transforms, image enhancement and restoration, segmentation, morphological processing, feature extraction, compression, and multiresolution analysis. The course develops the computational understanding required for applications such as machine vision, embedded vision, image-based inspection, and hardware-accelerated image processing.

Course Objectives

1. Understand and formulate fundamental mathematical models for digital image representation, sampling, quantization, color spaces, and frequency-domain transformations.
2. Apply and evaluate spatial and frequency-domain filtering techniques to effectively enhance degraded images and implement mathematical noise models for robust image restoration.
3. Analyze comprehensive methodologies for image segmentation, morphological feature isolation, boundary descriptors, and high-efficiency image compression algorithms suited for multiresolution visual data.

Unit I: Digital Image Fundamentals and Transforms **9 Hours**
Digital image processing systems and applications - Image sensing and acquisition - Image sampling and quantization - Pixel relationships: neighbourhood, adjacency, connectivity and distance measures - Colour image fundamentals: RGB, HSI and YUV models - Two-dimensional mathematical preliminaries - Two-dimensional Discrete Fourier Transform (2D DFT) - Properties and applications of 2D DFT - Discrete Cosine Transform (DCT).
Active Learning Activity: Perform sampling and quantization of representative images and analyze their effects on spatial resolution, intensity resolution, and image quality.

Unit II: Image Enhancement and Restoration **9 Hours**
Intensity transformations and contrast stretching - Histogram processing: equalization and specification - Spatial smoothing filters - Spatial sharpening filters - Frequency-domain filtering concepts - Ideal, Butterworth and Gaussian low-pass and high-pass filters - Image degradation and noise models - Mean and order-statistic filtering - Inverse and Wiener filtering.
Active Learning Activity: Compare spatial-domain and frequency-domain enhancement techniques for noisy and degraded images using suitable image-quality measures.

Unit III: Image Segmentation and Morphological Processing **9 Hours**
Detection of discontinuities: point, line and edge detection - Edge linking and boundary detection - Hough transform - Global thresholding - Adaptive thresholding - Region growing - Region splitting and merging - Morphological operations: erosion, dilation, opening and closing

- Morphological boundary extraction and watershed segmentation.
Active Learning Activity: Implement and compare edge-based, threshold-based, region-based, and morphological segmentation techniques on representative images.

Unit IV: Image Representation and Feature Extraction **9 Hours**
Image and boundary representation - Chain codes and boundary descriptors - Fourier descriptors - Region and geometric descriptors - Shape features and feature normalization - Texture analysis and statistical texture descriptors - Gray Level Co-occurrence Matrix (GLCM) - Feature matching - Introduction to pattern classes and image recognition.
Active Learning Activity: Extract shape and texture features from representative images and compare their effectiveness for basic image classification.

Unit V: Image Compression and Multiresolution Processing **9 Hours**
Fundamentals of image compression and redundancy - Coding, interpixel and psychovisual redundancies - Lossless and lossy compression - Run Length Encoding and Huffman coding - Arithmetic and predictive coding - Transform coding and JPEG - JPEG 2000 and wavelet-based compression - Multiresolution analysis and subband coding - Applications and performance evaluation of image compression.
Active Learning Activity: Compare lossless and lossy compression techniques using compression ratio and reconstructed image quality measures.

Course Outcomes

CO1: Apply digital image representation, sampling, quantization, colour models, and two-dimensional transform techniques to process digital images. (K3)
CO2: Apply spatial and frequency-domain enhancement and restoration techniques to improve degraded digital images. (K3)
CO3: Analyze edge detection, thresholding, region-based segmentation, and morphological techniques for extracting meaningful regions from digital images. (K4)
CO4: Analyze boundary, shape, and texture descriptors for extracting discriminative features from digital images. (K4)
CO5: Evaluate image compression and multiresolution techniques based on compression efficiency and reconstructed image quality. (K5)

Resources

1. Text Books

1. Gonzalez, R. C., & Woods, R. E. (2020). Digital image processing (4th ed.). Pearson.
2. Jain, A. K. (2022). Fundamentals of digital image processing. Pearson Education.
3. Sridhar, S. (2021). Digital image processing (3rd ed.). Oxford University Press.
4. Pratt, W. K. (2020). Digital image processing: PIKS scientific inside (4th ed.). Wiley.
5. Sonka, M., Hlavac, V., & Boyle, R. (2021). Image processing, analysis, and machine vision (4th ed.). Cengage Learning.

2. Reference Books

1. Bovik, A. C. (2021). The essential guide to image processing (2nd ed.). Academic Press.
2. Tekalp, A. M. (2020). Digital video processing (2nd ed.). Pearson.

3. Burger, W., & Burge, M. J. (2022). Digital image processing: An algorithmic introduction (3rd ed.). Springer.

4. Marques, O. (2020). Practical image and video processing (2nd ed.). Wiley-IEEE Press.

5. Russ, J. C., & Neal, F. B. (2021). The image processing handbook (8th ed.). CRC Press.

3. E-Resources

1. NPTEL. Digital Image Processing Fundamentals.
   `https://nptel.ac.in/courses/117105079`
2. NPTEL. Image Processing and Computer Vision Applications.
   `https://nptel.ac.in/courses/106105032`
3. NPTEL. Multiresolution Image Processing and Wavelets.
   `https://nptel.ac.in/courses/117101123`
4. OpenCV Documentation and Image Analysis Tutorials.
   `https://docs.opencv.org/master/`
5. IEEE Signal Processing Society Educational Resources Center.
   `https://signalprocessingsociety.org/education-resources`

Industrial Relevance

Digital image processing is fundamental to machine vision, semiconductor inspection, medical imaging, autonomous systems, surveillance, consumer electronics, remote sensing, and embedded vision. Image enhancement, segmentation, feature extraction, and compression algorithms are widely implemented in embedded processors, DSPs, GPUs, FPGAs, and dedicated VLSI accelerators. The course provides the robust algorithmic foundation required for engineering efficient, hardware-accelerated image-processing and intelligent embedded-vision systems within the global semiconductor and electronic design automation industry.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	1	2	-	-	1	1	-	2	3	2	2
CO2	3	3	2	2	3	-	-	1	1	-	2	3	2	2
CO3	3	3	3	3	3	-	-	1	1	1	2	3	3	2
CO4	3	3	3	3	3	-	-	1	1	1	2	3	2	2
CO5	3	3	3	3	3	-	-	1	2	1	2	3	3	3
Weighted Average	3.00	2.80	2.60	2.40	2.80	-	-	1.00	1.20	1.00	2.00	3.00	2.40	2.20

Course Code: U23EVV58
Course Title: COMPUTER VISION FOR EMBEDDED SYSTEMS
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
SDG: 9
Prerequisites: Digital Signal Processing Algorithms

Course Overview

This course introduces the foundational principles and algorithms of computer vision with a specialized focus on deployment within resource-constrained embedded and edge-computing platforms. It systematically covers image formation, geometric alignment, motion estimation, and deep-learning-based visual recognition techniques essential for modern hardware implementation. By exploring model quantization and hardware-aware optimization, the curriculum ensures students can effectively engineer and deploy robust vision applications on specialized semiconductor architectures.

Course Objectives

1. Analyze image formation, camera geometry, and feature representation algorithms to construct reliable visual representations from raw sensor data.
2. Implement geometric transformations, motion estimation, and object tracking methodologies to extract critical spatial and temporal information from dynamic image sequences.
3. Evaluate and optimize deep-learning vision models using hardware-aware quantization and pruning techniques for highly efficient deployment on resource-constrained embedded platforms.

Unit I: Image Formation and Feature Representation **9 Hours**
Computer vision pipeline and applications - Image formation and pinhole camera model - Camera parameters and coordinate systems - Coordinate transformations and camera calibration - Geometric primitives and image features - Interest points and corner detection - Harris corner detector - Scale-invariant feature descriptors - Feature matching and descriptor distance measures.
Active Learning Activity: Detect local features in images acquired from different viewpoints and match the corresponding features using suitable feature descriptors.
Unit II: Geometric Vision and Image Alignment **9 Hours**
Two-dimensional geometric transformations - Translation, Euclidean and affine transformations - Projective transformations and homogeneous coordinates - Feature correspondence - Homography estimation - Direct and feature-based image alignment - Robust model fitting and consensus-based estimation - Image registration - Image stitching and panorama generation.
Active Learning Activity: Estimate a homography from matched image features and use it to perform image registration or panorama generation using open-source scientific computing libraries.
Unit III: Motion, Stereo and Object Tracking **9 Hours**
Image sequences and motion representation - Optical flow fundamentals - Differential optical-flow estimation methods - Motion estimation - Background modeling and subtraction - Object tracking and feature-based tracking - Stereo vision fundamentals - Epipolar geometry and stereo correspondence - Disparity and depth estimation including an introduction to structure from motion.

Active Learning Activity: Implement motion estimation or object tracking on a video sequence and analyze the effect of motion and scene characteristics on tracking performance.

Unit IV: Visual Recognition and Deep Vision **9 Hours**

Image classification and visual recognition - Feature-based recognition and machine-learning approaches - Convolutional Neural Network fundamentals - Convolution, pooling and feature maps - Transfer learning for visual recognition - Object detection fundamentals - Region-based and single-stage object detection concepts - Semantic image segmentation - Vision performance metrics including accuracy, precision, recall, F-score, intersection over union and mean average precision.

Active Learning Activity: Develop and evaluate a basic image-classification or object-detection application using transfer learning methodologies and compute appropriate performance metrics.

Unit V: Embedded Computer Vision **9 Hours**

Embedded computer-vision architecture - Camera and processor interfacing - Resource constraints encompassing computation, memory, latency and power - Edge inference and lightweight vision models - Model quantization - Model pruning and knowledge-distillation concepts - Hardware-aware optimization - CPU, GPU and NPU-based vision processing utilizing lightweight interoperable machine learning frameworks - Real-time performance evaluation and embedded vision applications.

Active Learning Activity: Evaluate a lightweight vision model on an embedded or edge computing platform and critically analyze the architectural trade-offs among accuracy, inference latency, memory footprint, and power consumption.

Course Outcomes

CO1: Apply camera geometry, calibration, feature detection, and feature description techniques to establish visual representations from complex image data. (K3)

CO2: Apply geometric transformations, feature matching, homography estimation, and robust estimation techniques for precise image alignment and registration. (K3)

CO3: Analyze optical flow, motion estimation, stereo vision, and object-tracking techniques for extracting motion and depth information from multi-dimensional image sequences. (K4)

CO4: Analyze convolutional neural networks and deep-learning-based techniques for advanced image classification, object detection, and semantic segmentation in vision pipelines. (K4)

CO5: Evaluate and optimize computer vision models utilizing quantization, pruning, and hardware-aware structural techniques specifically for resource-constrained embedded and edge computing platforms. (K5)

Resources

1. Text Books

1. Szeliski, R. (2022). *Computer Vision: Algorithms and Applications* (2nd ed.). Springer.
2. Elgendy, M. (2020). *Deep Learning for Vision Systems.* Manning Publications.
3. Prince, S. J. D. (2023). *Understanding Deep Learning.* MIT Press.
4. Forsyth, D. A., & Ponce, J. (2019). *Computer Vision: A Modern Approach* (2nd ed.). Pearson.
5. Gonzalez, R. C., & Woods, R. E. (2020). *Digital Image Processing* (4th ed.). Pearson.

2. Reference Books

1. Hartley, R., & Zisserman, A. (2021). *Multiple View Geometry in Computer Vision* (2nd ed.). Cambridge University Press.
2. Bradski, G., & Kaehler, A. (2019). *Learning Computer Vision Fundamentals*. O'Reilly Media.
3. Goodfellow, I., Bengio, Y., & Courville, A. (2020). *Deep Learning*. MIT Press.
4. Aggarwal, C. C. (2022). *Neural Networks and Deep Learning: A Textbook*. Springer.
5. Khan, S., Rahmani, H., Shah, S. A. A., & Bennamoun, M. (2021). *A Guide to Convolutional Neural Networks for Computer Vision*. Morgan & Claypool.

3. E-Resources

1. NPTEL. (2022). Image Formation and Camera Geometry [Video course]. `https://nptel.ac.in/courses/106105216`
2. NPTEL. (2021). Deep Learning for Computer Vision Applications [Video course]. `https://nptel.ac.in/courses/106106224`
3. Open Source Vision Consortium. (2023). Computer Vision Documentation and Tutorials. `https://docs.opensourcevision.org`
4. Embedded Machine Learning. (2023). Lightweight Model Deployment Guide. `https://embedded-ml.org/deployment`
5. Open Neural Network Exchange. (2022). Interoperable Machine Learning Models. `https://onnx.ai/resources`

Industrial Relevance

Computer vision serves as the fundamental perceptual backbone for modern industrial automation, autonomous navigation, and intelligent edge-computing devices. As the global semiconductor industry pivots towards specialized Application-Specific Integrated Circuits (ASICs) and edge-AI accelerators, there is a critical engineering demand for vision algorithms that satisfy stringent hardware constraints regarding latency, power consumption, and thermal limits. By mastering camera geometry, feature extraction, and hardware-aware neural network optimization—including deep model quantization and pruning—students bridge the gap between theoretical visual computation and highly efficient silicon deployment. This embedded-centric pedagogical approach ensures readiness for technical roles involving SoCs, dedicated vision NPUs, and next-generation VLSI architectures within the semiconductor sector.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	1	2	-	-	-	-	-	2	3	2	2
CO2	3	3	3	2	3	-	-	-	1	-	2	3	2	3
CO3	3	3	3	3	3	-	-	-	1	-	2	3	2	3
CO4	3	3	3	3	3	-	-	1	1	1	2	3	3	3
CO5	3	3	3	3	3	1	-	1	1	1	2	3	3	3
Weighted Average	3.00	2.80	2.80	2.40	2.80	1.00	-	1.00	1.00	1.00	2.00	3.00	2.40	2.80

Course Code: U23EVV59
Course Title: FPGA-BASED IMAGE AND VIDEO PROCESSING
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design, SystemVerilog
SDG: 9

Course Overview

This course provides a comprehensive exploration of designing Field Programmable Gate Array (FPGA) architectures specifically tailored for real-time image and video processing applications. Students will investigate parallel processing paradigms, streaming architectures, and hardware-software co-design to accelerate computationally intensive computer vision algorithms effectively. Ultimately, the curriculum bridges theoretical image processing concepts with practical semiconductor industry deployment workflows to optimize resource utilization, latency, and power in embedded vision systems.

Course Objectives

1. Formulate hardware architectures exploiting data-level and task-level parallelism for fundamental image and video processing operations.
2. Design high-throughput, low-latency streaming pipelines using standard interfaces and memory abstraction techniques suitable for real-time video workloads.
3. Evaluate and optimize hardware accelerators for advanced computer vision algorithms using Register Transfer Level and High-Level Synthesis design methodologies.

Unit I: FPGA ARCHITECTURES FOR VISION PROCESSING 9 Hours
FPGA-based image and video processing architectures - FPGA resources: LUTs, flip-flops, Block RAM and DSP slices - Software versus hardware implementation - Data-level and task-level parallelism - Pipelining, latency and throughput - Fixed-point representation and quantization - Word-length optimization - Streaming architectures and line/frame buffering - Memory bandwidth and hardware/software partitioning.
Active Learning Activity: Convert a representative image-processing operation from floating-point to fixed-point representation and analyze the effects on accuracy, resource utilization, and computational complexity.

Unit II: HARDWARE ARCHITECTURES FOR IMAGE PROCESSING 9 Hours
Pixel-level processing architectures - Point operations and color-space conversion - Histogram computation architecture - Convolution and sliding-window architectures - Line-buffer-based image processing - Spatial filtering and Gaussian filtering - Sobel edge-detection architecture - Canny edge-detection architecture - Morphological processing and resource optimization.
Active Learning Activity: Design a pipelined Sobel edge-detection architecture using RTL or HLS and analyze its latency, throughput, and FPGA resource utilization.

Unit III: REAL-TIME VIDEO PROCESSING ARCHITECTURES 9 Hours
Digital video fundamentals and pixel-stream representation - Video formats, frame rate and pixel-clock requirements - Streaming video architecture - Video buffering and line/frame buffers - Color-space conversion for video streams - Image resizing and interpolation - Video scaling and frame-rate conversion concepts - AXI4-Stream and memory-mapped video interfaces - DMA

and real-time video-processing pipelines.
Active Learning Activity: Develop a streaming video-processing pipeline incorporating color conversion, filtering, and edge detection, and analyze its real-time throughput.

Unit IV: HARDWARE ACCELERATION OF COMPUTER VISION 9 Hours
Hardware architectures for feature detection - Harris corner-detector acceleration - Hardware architectures for motion estimation - Optical-flow acceleration - Stereo-vision and disparity-estimation architectures - Object-detection preprocessing architectures - Convolution and parallel Multiply-Accumulate (MAC) architectures - FPGA-based CNN acceleration fundamentals - Hardware architecture trade-offs for real-time computer vision.
Active Learning Activity: Design and analyze a hardware accelerator for a selected feature-detection, optical-flow, stereo, or convolution operation using structural RTL or HLS.

Unit V: FPGA VISION SYSTEM DESIGN AND OPTIMIZATION 9 Hours
RTL-based and HLS-based vision-system design - HLS design methodology using C/C++ - Loop pipelining and loop unrolling - Array partitioning and dataflow optimization - FPGA IP-core generation and integration - AXI interface integration and SoC FPGA architecture - Processor–FPGA communication and hardware/software co-design - Resource utilization, timing, latency and throughput analysis - Power-performance optimization and FPGA vision-system case studies.
Active Learning Activity: Implement an image/video-processing accelerator using HLS, generate an FPGA IP core, and evaluate resource utilization, latency, throughput, and power-performance trade-offs.

Course Outcomes (CO)

CO1: Apply FPGA architectural resources, parallel-processing principles, fixed-point representation, and streaming concepts to formulate real-time vision-processing architectures. (K3)
CO2: Develop pipelined and parallel hardware architectures for pixel-level, filtering, edge-detection, and morphological image-processing operations. (K3)
CO3: Develop streaming video-processing architectures using buffering, video interfaces, and DMA mechanisms for real-time operation. (K3)
CO4: Analyze hardware architectures and resource-optimization techniques for accelerating computationally intensive computer-vision algorithms on FPGAs. (K4)
CO5: Evaluate FPGA-based vision systems using RTL/HLS methodologies with respect to resource utilization, timing, latency, throughput, and power-performance trade-offs. (K5)

Resources

1. Text Books

1. Bailey, D. G. (2023). *Design for Embedded Image Processing on FPGAs* (2nd ed.). Wiley-IEEE Press.

2. Woods, R., McAllister, J., Lightbody, G., & Yi, Y. (2020). *FPGA-Based Implementation of Signal Processing Systems* (2nd ed.). Wiley.

3. Szeliski, R. (2022). *Computer Vision: Algorithms and Applications* (2nd ed.). Springer.

4. Meyer-Baese, U. (2019). *Digital Signal Processing with Field Programmable Gate Arrays* (4th ed.). Springer.

5. Gonzalez, R. C., & Woods, R. E. (2020). *Digital Image Processing* (4th ed.). Pearson.

2. Reference Books

1. Maxfield, C. (2019). *The Design Warrior's Guide to FPGAs: Devices, Tools and Flows.* Elsevier.
2. Wolf, W. (2021). *FPGA-Based System Design: Modern Architectures and Methodologies.* Pearson.
3. Coussy, P., & Morawiec, A. (2019). *High-Level Synthesis: From Algorithm to Digital Circuit.* Springer.
4. Sadrozinski, H. F.-W., & Wu, J. (2020). *Applications of Field-Programmable Gate Arrays in Scientific Research.* Taylor & Francis.
5. Ashenden, P. J. (2021). *Digital Design: An Embedded Systems Approach Using SystemVerilog.* Morgan Kaufmann.

3. E-Resources

1. NPTEL. (2022). Architectures for Digital Signal Processing. Note: Covers pipelining, parallelism, and hardware design concepts.
   `https://nptel.ac.in/courses/117102060`
2. NPTEL. (2021). Digital Image Processing. Note: Fundamentals of spatial filtering and morphological operations.
   `https://nptel.ac.in/courses/117105079`
3. NPTEL. (2023). Hardware Modeling using Verilog. Note: RTL design principles and structural modeling fundamentals.
   `https://nptel.ac.in/courses/106105165`
4. IEEE Xplore. (2023). FPGA-based image/video processing and hardware acceleration research. Note: Academic publications on High-Level Synthesis and architectures.
   `https://ieeexplore.ieee.org/`
5. OpenCores. (2023). Open-source hardware IP and FPGA design resources. Note: Practical engineering implementations of image processing Intellectual Property.
   `https://opencores.org/`

Industrial Relevance

FPGA-based image and video processing is extensively deployed across advanced industrial sectors, including automotive Advanced Driver Assistance Systems (ADAS), autonomous robotics, medical imaging, and edge-computing surveillance networks. Because these domains require deterministic latency and extremely high throughput that traditional microprocessors cannot achieve, engineers utilize custom hardware architectures to accelerate critical vision tasks. This course directly aligns with contemporary semiconductor and embedded-system workflows by bridging the gap between theoretical algorithms and physical hardware implementation, equipping graduates with the RTL design, streaming pipeline, and IP integration skills actively demanded by global hardware technology companies.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	1	3	-	-	-	-	-	2	3	3	2
CO2	3	3	3	2	3	-	-	-	1	-	2	3	3	2
CO3	3	3	3	2	3	-	-	-	1	-	2	3	3	2
CO4	3	3	3	3	3	-	-	-	1	-	2	3	3	3
CO5	3	3	3	3	3	1	-	1	1	1	3	3	3	3
Weighted Average	3.00	2.80	2.80	2.20	3.00	1.00	-	1.00	1.00	1.00	2.20	3.00	3.00	2.40

Course Code: U23EVV60
Course Title: CMOS IMAGE SENSORS AND CAMERA SYSTEMS
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisite: CMOS Integrated Circuits
SDG: 9

Course Overview

This course introduces the fundamental principles, architectures, and performance parameters of solid-state image sensors and integrated camera systems. It systematically covers the complete imaging pipeline, spanning from photodetection mechanisms and CMOS pixel architectures to advanced readout circuits and image signal processing algorithms. The curriculum equips students with the specialized analytical and system-level design skills required to evaluate and develop low-power, high-performance imaging solutions for modern mobile, automotive, and industrial embedded applications.

Course Objectives

1. Analyze the fundamental photodetection mechanisms, pixel architectures, and noise models inherent in modern CMOS image sensors.
2. Evaluate the design and performance trade-offs of readout circuits, data converters, and image signal processing pipelines used in embedded camera systems.
3. Characterize integrated camera system architectures, interface protocols, and emerging depth-sensing technologies for specialized industrial and automotive vision applications.

Unit I: Image Sensor Fundamentals **9 Hours**
Solid-state imaging principles and image formation - Photodetectors and photodiodes - Photoelectric conversion and charge generation - Quantum efficiency and responsivity - Dark current and temperature effects - Noise sources in image sensors - Dynamic range and signal-to-noise ratio - CCD and CMOS image sensors - Image sensor performance parameters.
Active Learning Activity: Analyze the effect of temperature and illumination on photodiode responsivity, dark current, noise and signal-to-noise ratio using a suitable device-level simulation environment.

Unit II: CMOS Pixel Architectures **9 Hours**
CMOS image sensor architecture and pixel array organization - Passive Pixel Sensor and Active Pixel Sensor - 3T and 4T CMOS pixel architectures - Pinned photodiode and charge-transfer mechanism - Reset, source-follower and row-select circuits - Correlated Double Sampling (CDS) - Fixed Pattern Noise and pixel-level noise mechanisms - Rolling-shutter and global-shutter operation - Pixel scaling, fill factor and pixel design trade-offs.
Active Learning Activity: Compare 3T and 4T CMOS active-pixel architectures and analyze their charge-transfer, noise and CDS characteristics using a standard circuit simulation environment.

Unit III: Readout and Data Conversion Circuits **9 Hours**
CMOS image-sensor readout architecture - Row and column addressing and readout - Column

amplifiers and programmable-gain amplifiers - Sample-and-hold circuits - Column-parallel ADC architecture - Single-slope ADC for image sensors - SAR ADC concepts for image sensors - Timing, control and noise-reduction circuits - Sensor output interfaces and data-converter trade-offs.
Active Learning Activity: Develop a behavioral model of a column-parallel single-slope ADC readout chain and analyze speed, resolution, noise and power trade-offs.

Unit IV: Image Signal Processing Pipeline **9 Hours**
Image Signal Processor (ISP) architecture - Color Filter Array and Bayer pattern - Demosaicing - Black-level and defective-pixel correction - Lens-shading correction and sensor-noise reduction - White balance and color correction - Gamma correction and edge enhancement - High Dynamic Range imaging - Auto exposure, auto white balance and auto-focus concepts.
Active Learning Activity: Process raw Bayer-pattern sensor data and implement basic demosaicing, defective-pixel correction and auto-exposure operations using an appropriate image processing environment.

Unit V: Camera Systems and Applications **9 Hours**
Integrated camera-system architecture - Optics, image-sensor integration and camera control - Sensor output and camera interfaces - MIPI CSI concepts - Camera modules and multi-camera systems - Depth-sensing fundamentals - Time-of-Flight imaging - Event-based vision sensor concepts - Low-power camera systems and emerging applications.
Active Learning Activity: Analyze a multi-camera or Time-of-Flight camera architecture for an automotive or embedded-vision application and evaluate sensor interface, bandwidth, power and system-level design considerations.

Course Outcomes (COs)

1. CO1: Apply the operating principles, photodetection mechanisms and performance parameters of solid-state image sensors to characterize CMOS imaging systems. (K3)
2. CO2: Analyze CMOS pixel architectures, charge-transfer mechanisms, noise sources and shutter techniques to evaluate pixel-level performance. (K4)
3. CO3: Analyze image-sensor readout and data-conversion circuits with respect to speed, noise, resolution and power requirements. (K4)
4. CO4: Apply image signal processing techniques to correct sensor artifacts and improve the quality and dynamic range of captured images. (K3)
5. CO5: Evaluate integrated camera architectures, interfaces and emerging imaging technologies for mobile, automotive, industrial and embedded applications. (K5)

Resources

1. Text Books

1. Kuroda, T. (2021). Essential Principles of Image Sensors. CRC Press.
2. Ohta, J. (2020). Smart CMOS Image Sensors and Applications (2nd ed.). CRC Press.
3. Theuwissen, A. J. P. (2022). Solid-State Imaging with Charge-Coupled and CMOS Devices. Springer.

4. Sze, S. M., & Lee, M. K. (2021). Semiconductor Devices: Physics and Technology (4th ed.). Wiley.

5. Gonzalez, R. C., & Woods, R. E. (2020). Digital Image Processing (4th ed.). Pearson.

2. Reference Books

1. Nakamura, J. (2019). Image Sensors and Signal Processing for Digital Still Cameras. Taylor & Francis.

2. Holst, G. C., & Lomheim, T. S. (2022). CMOS/CCD Sensors and Camera Systems (3rd ed.). JCD Publishing.

3. Seitz, P., & Theuwissen, A. J. P. (2020). Single-Photon Imaging. Springer.

4. Vinet, P. (2021). Automotive Imaging and Advanced Driver Assistance Systems. Elsevier.

5. Durini, D. (2019). High Performance Silicon Imaging: Fundamentals and Applications of CMOS and CCD Sensors (2nd ed.). Woodhead Publishing.

3. E-Resources

1. NPTEL. (2023). VLSI Data Conversion Circuits.
`https://nptel.ac.in/courses/108105105`

2. MIT OpenCourseWare. (2021). Solid-State Imaging Systems.
`https://ocw.mit.edu/`

3. IEEE Xplore Digital Library. (2023). Advanced CMOS Image Sensors and Imaging Systems.
`https://ieeexplore.ieee.org/`

4. NPTEL. (2022). Digital Image Processing and Sensor Pipelines.
`https://nptel.ac.in/courses/117105079`

5. ACM Digital Library. (2023). Event-Based Vision and Time-of-Flight Imaging.
`https://dl.acm.org/`

Industrial Relevance

CMOS image sensors serve as the critical foundational components for modern mobile cameras, advanced driver-assistance systems (ADAS), autonomous vehicles, industrial machine vision, and medical diagnostic equipment. Developing advanced imaging Systems-on-Chip (SoCs) requires the rigorous integration of highly sensitive photodetectors, specialized analog readout circuits, precise analog-to-digital converters, and efficient signal processing engines. This curriculum thoroughly prepares engineering professionals with the requisite system-level design methodologies and architectural analytical skills demanded by leading semiconductor manufacturers and embedded systems developers to innovate next-generation low-power, high-speed visual computing platforms.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	2	-	-	-	-	-	2	3	1	2
CO2	3	3	3	3	3	-	-	1	1	-	2	3	3	2
CO3	3	3	3	3	3	-	-	-	-	-	2	3	2	3
CO4	3	2	3	2	3	-	-	1	1	-	2	3	1	2
CO5	3	3	3	3	3	1	1	1	1	1	2	3	2	3
Weighted Average	3.00	2.80	2.80	2.60	2.80	1.00	1.00	1.00	1.00	1.00	2.00	3.00	1.80	2.40

Course Code: U23EVV61
Course Title: AI ACCELERATORS FOR VISION SYSTEMS
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital Signal Processing Algorithms
SDG: 9

Course Overview

This course introduces specialized hardware architectures designed to accelerate artificial intelligence and deep-learning workloads in modern vision systems. It provides a comprehensive analysis of neural-network computational patterns, processing-element arrays, dataflow strategies, and memory hierarchies essential for energy-efficient hardware implementations. Students will explore hardware-software co-design principles across various deployment platforms to optimize real-time vision applications.

Course Objectives

1. To analyze the computational characteristics and architectural building blocks of artificial intelligence workloads for vision systems.
2. To evaluate dataflow strategies, memory hierarchies, and reduced-precision arithmetic techniques that optimize energy efficiency and data reuse.
3. To assess different hardware implementations, including application-specific and programmable accelerators, using comprehensive performance metrics.

Unit I: AI ACCELERATOR ARCHITECTURE FUNDAMENTALS 9 Hours
AI workloads and computational characteristics - Neural-network operations: convolution and matrix multiplication - Parallelism in AI workloads - Processing Elements (PEs) and MAC units - Processing-element arrays - SIMD and vector architectures - Systolic-array architectures - AI accelerator microarchitecture - Performance metrics: throughput, latency, utilization and efficiency.
Active Learning Activity: Model a two-dimensional processing-element array for matrix multiplication and evaluate its throughput and PE utilization.

Unit II: NEURAL NETWORK COMPUTE ARCHITECTURES 9 Hours
Convolutional neural-network computational mapping - Convolution-to-matrix-multiplication mapping - MAC-array architectures - Matrix-multiplication engines - Depthwise and pointwise convolution architectures - Pipelined compute architectures - Loop tiling and loop unrolling - Parallelism and workload scheduling - Accelerator microarchitecture design trade-offs.
Active Learning Activity: Compare alternative convolution mappings and loop-unrolling strategies and evaluate their effects on PE utilization and execution latency.

Unit III: DATAFLOW AND MEMORY ARCHITECTURES 9 Hours
Dataflow architectures for AI accelerators - Weight-stationary dataflow - Output-stationary dataflow - Row-stationary dataflow - Activation and weight reuse - Memory hierarchy in AI accelerators - On-chip SRAM buffers and tiling - Double buffering and bandwidth management - Data movement and off-chip memory optimization.
Active Learning Activity: Compare weight-stationary, output-stationary, and row-stationary dataflows in terms of data reuse, memory traffic, and energy consumption.

Unit IV: ENERGY-EFFICIENT AI ACCELERATOR DESIGN **9 Hours**
Reduced-precision arithmetic for AI workloads - Floating-point and fixed-point representations - Quantization and quantization error - Low-precision datapath architectures - Sparsity in neural networks - Zero-skipping and sparse computation - Compute-memory trade-offs - Clock and power considerations - Energy-efficiency and accelerator performance metrics.
Active Learning Activity: Analyze the accuracy, hardware-resource, and energy implications of reduced-precision arithmetic and sparsity-aware computation.

Unit V: FPGA, ASIC AND NPU ACCELERATOR ARCHITECTURES 9 Hours
FPGA-based AI accelerator architectures - ASIC-based AI accelerator architectures - Neural Processing Unit (NPU) architectures - Heterogeneous AI accelerator SoCs - High-Level Synthesis (HLS) for AI accelerators - Hardware-software interface and accelerator integration - Accelerator benchmarking and design-space exploration - Performance, area, latency and power trade-offs - Vision-AI accelerator architecture case studies.
Active Learning Activity: Develop a high-level synthesis based convolution accelerator model and evaluate resource utilization, latency, throughput, and power-performance trade-offs.

Course Outcomes (COs)

CO1: Apply the computational characteristics and parallelism of vision-AI workloads to formulate processing-element arrays and systolic architectures. (K3)

CO2: Analyze convolution and matrix-multiplication mappings, pipelining, and loop transformations for neural-network accelerator architectures. (K4)

CO3: Analyze dataflow strategies and memory hierarchies to optimize data reuse, bandwidth, and data movement in AI accelerators. (K4)

CO4: Evaluate quantization, reduced-precision arithmetic, and sparsity-aware architectures for energy-efficient AI acceleration. (K5)

CO5: Evaluate FPGA, ASIC, and NPU accelerator architectures using throughput, latency, area, memory bandwidth, and energy-efficiency metrics. (K5)

Resources

1. Text Books

1. Sze, V., Chen, Y.-H., Yang, T.-J., & Emer, J. S. (2020). Efficient processing of deep neural networks. Morgan & Claypool.
2. Hennessy, J. L., & Patterson, D. A. (2019). Computer architecture: A quantitative approach (6th ed.). Morgan Kaufmann.
3. Mishra, A., & Gupta, S. (2022). Hardware accelerators for machine learning. Springer.
4. Wolf, W. (2021). High-performance embedded computing: Architectures, applications, and methodologies (2nd ed.). Elsevier.
5. Jouppi, N. P., et al. (2023). Domain-specific architectures for deep learning. IEEE Press.

2. Reference Books

1. Li, H., & Chen, Y. (2020). Edge AI: Hardware architecture and implementations. Wiley.
2. Wang, Y., & Zhang, Z. (2021). Energy-efficient neural network accelerators. Cambridge University Press.
3. Qiao, Y., & Liu, H. (2022). FPGA-based artificial intelligence acceleration. Artech House.
4. Smith, J., & Nair, R. (2019). Virtual machines and domain-specific hardware. Morgan Kaufmann.
5. Pedram, M., & Hwang, E. (2023). Low-power design for edge computing systems. Springer.

3. E-Resources

1. NPTEL. (2022). High-performance computer architecture and AI acceleration [Video series].
   `https://nptel.ac.in/courses/106105220`
2. MIT OpenCourseWare. (2020). Hardware architecture for deep learning [Course materials].
   `https://ocw.mit.edu/courses/eecs/deep-learning-hardware`
3. IEEE Computer Society. (2023). Domain-specific AI accelerators tutorial [Documentation].
   `https://www.computer.org/education/ai-accelerators`
4. ACM Digital Library. (2021). Accelerator architecture and benchmarking guide [Web portal].
   `https://dl.acm.org/special-interest-groups/sigarch`
5. Coursera. (2022). Edge AI and hardware acceleration [Online course].
   `https://www.coursera.org/learn/edge-ai-hardware`

Industrial Relevance

AI accelerators are increasingly deployed in autonomous vehicles, robotics, smart cameras, and edge computing platforms to meet stringent real-time processing demands. Specialized architectures, such as systolic arrays and spatial dataflow engines, address the severe memory-bandwidth and energy constraints inherent in neural-network inference. This course develops critical skills in architecture exploration, hardware-software co-design, and performance benchmarking, directly aligning with current practices in the global semiconductor industry for developing energy-efficient edge and high-performance computing solutions.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	2	–	–	–	–	–	2	3	2	2
CO2	3	3	3	2	3	–	–	–	1	–	2	3	3	2
CO3	3	3	3	3	3	–	–	–	1	–	2	3	3	3
CO4	3	3	3	3	3	–	–	–	1	1	2	3	3	3
CO5	3	3	3	3	3	1	–	1	1	1	3	3	3	3
Weighted Average	3.00	3.00	2.80	2.60	2.80	1.00	–	1.00	1.00	1.00	2.20	3.00	2.80	2.60

Course Code: U23EVV62
Course Title: EDGE AI VISION SYSTEMS
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital Signal Processing Algorithms
SDG: 9

Course Overview

This course introduces the architecture, optimization, deployment, and real-time execution of artificial intelligence-based vision systems on resource-constrained edge platforms. It comprehensively covers edge-versus-cloud architectures, lightweight neural networks, model conversion workflows, and real-time embedded vision pipelines. Emphasis is strategically placed on hardware-software co-design to balance latency, memory, bandwidth, and power for application-specific intelligent systems in the semiconductor and embedded industries.

Course Objectives

The course enables students to:

1. Understand edge-AI vision architectures and evaluate the trade-offs between cloud and edge-based inference for real-time systems.
2. Apply neural-network optimization techniques including quantization, pruning, and knowledge distillation for resource-constrained edge hardware platforms.
3. Analyze real-time embedded vision pipelines using performance metrics to deploy and profile application-specific intelligent edge systems.

Unit I: EDGE AI VISION SYSTEM ARCHITECTURE **9 Hours**
Introduction to Edge AI and intelligent vision systems - Cloud computing and edge computing architectures - Edge versus cloud inference - Camera-to-inference pipeline - Latency and response-time requirements - Bandwidth and data-transfer constraints - Power and energy considerations - Privacy and security considerations in edge vision - Embedded Edge-AI system architecture.
Active Learning Activity: Analyze a camera-to-inference pipeline and compare cloud and edge implementations based on latency, bandwidth, power, privacy, and response time.

Unit II: NEURAL NETWORK OPTIMIZATION FOR EDGE DEPLOYMENT 9 Hours
Computational and memory characteristics of vision neural networks - Lightweight neural-network architectures - Model compression techniques - Post-training quantization - Quantization-aware training concepts - Neural-network pruning - Structured and unstructured sparsity - Knowledge distillation - Hardware-aware model optimization and accuracy-resource trade-offs.
Active Learning Activity: Compare a floating-point vision model with a quantized and pruned version and analyze model size, computational complexity, accuracy, and inference latency.

Unit III: EMBEDDED AI PLATFORMS AND TOOLCHAINS **9 Hours**
Embedded AI computing platforms - Microcontroller-based AI systems - Microprocessor and SoC-based AI systems - CPU, GPU and NPU execution - Lightweight neural-network inference

engines - Neural-network model exchange formats - Model conversion and optimization workflow - Embedded AI runtime environments - End-to-end edge-AI deployment workflow.
Active Learning Activity: Convert a trained vision model into an appropriate intermediate representation and develop an embedded deployment workflow considering memory, computation, and runtime constraints.

Unit IV: REAL-TIME EDGE VISION DEPLOYMENT 9 Hours
Real-time camera acquisition - Image and video preprocessing - Embedded model inference - Object classification and detection deployment - Real-time scheduling - Memory management and data movement - Frame rate and latency analysis - Performance profiling and bottleneck identification - Power-aware edge inference.
Active Learning Activity: Profile an embedded object-detection pipeline and evaluate FPS, latency, memory utilization, computational load, and power consumption.

Unit V: EDGE VISION APPLICATIONS AND INTELLIGENT SYSTEMS 9 Hours
Edge vision for automotive systems - Edge vision for robotics and autonomous systems - Industrial inspection and machine vision - Smart surveillance and IoT vision - Agricultural and environmental vision applications - Healthcare and assistive vision systems - TinyML-based vision systems - Edge-cloud collaborative intelligence - Privacy-preserving edge intelligence and system-level case studies.
Active Learning Activity: Design an application-specific edge-vision architecture by selecting the camera, processing platform, AI model, memory architecture, communication mechanism, and privacy strategy for a representative industrial or automotive application.

Course Outcomes (COs)

On successful completion of the course, students will be able to:

CO1: Analyze edge and cloud vision architectures and their latency, bandwidth, power, and privacy trade-offs. (K4)

CO2: Apply quantization, pruning, knowledge distillation, and model-compression techniques to optimize vision models for resource-constrained edge platforms. (K3)

CO3: Apply embedded CPU, GPU, NPU, model-conversion, and runtime tools to deploy optimized vision models on edge platforms. (K3)

CO4: Analyze real-time edge-vision pipelines using frame rate, latency, memory utilization, bandwidth, and power-performance metrics. (K4)

CO5: Evaluate and design application-specific edge-AI vision systems considering computational resources, energy, real-time performance, privacy, and system-level constraints. (K5)

Resources

1. Text Books

1. Situnayake, D., & Plunkett, L. (2023). *AI at the Edge: Solving Real-World Problems with Embedded Machine Learning*. O'Reilly Media.

2. Sze, V., Chen, Y.-H., Yang, T.-J., & Emer, J. S. (2020). *Efficient Processing of Deep Neural Networks*. Morgan & Claypool.

3. Shafique, M., & Theocharides, T. (Eds.). (2021). *Robust and Energy-Efficient Computing for Edge Intelligence*. Springer.

4. Warden, P., & Situnayake, D. (2019). *TinyML: Machine Learning with TensorFlow Lite on Arduino and Ultra-Low-Power Microcontrollers*. O'Reilly Media.

5. Li, H., & Chen, Y. (2022). *Deep Learning for Edge Computing Techniques and Applications*. CRC Press.

2. Reference Books

1. Reagen, B., Adolf, R., Whatmough, P., Thakur, S., & Brooks, D. (2019). *Deep Learning for Computer Vision: Architectural Design and Hardware Optimization*. Morgan & Claypool.

2. Merenda, M., Porcaro, C., & Iero, D. (2020). *Edge Machine Learning for the Internet of Things*. MDPI.

3. Wang, X., & Li, Y. (2021). *Edge Intelligence in the Making: Optimization, Deep Learning, and Applications*. Morgan & Claypool.

4. Zhou, Z., & Chen, X. (2022). *Edge AI: Convergence of Edge Computing and Artificial Intelligence*. Springer.

5. Cass, S. (2023). *Embedded AI: Hardware Accelerators for Machine Learning*. IEEE Press.

3. E-Resources

1. NPTEL. (2023). *Deep Learning for Visual Computing*.
`https://nptel.ac.in/courses/106106184`

2. MIT OpenCourseWare. (2020). *Efficient Deep Learning Computing*.
`https://ocw.mit.edu/courses/efficient-deep-learning-computing`

3. ARM Developer. (2023). *Embedded Machine Learning Resources*.
`https://developer.arm.com/solutions/machine-learning-on-arm`

4. NPTEL. (2021). *Embedded Systems Design*.
`https://nptel.ac.in/courses/108105057`

5. IEEE Xplore. (2023). *Edge Intelligence and Low-Power AI Hardware*.
`https://ieeexplore.ieee.org/Xplore/home.jsp`

Industrial Relevance

Edge AI is increasingly deployed across automotive advanced driver-assistance systems, robotics, industrial inspection, smart cameras, and autonomous IoT sensor networks. Unlike cloud-based inference, these edge systems must operate under strict hardware constraints regarding latency, memory bandwidth, thermal budgets, and energy consumption while ensuring data privacy. This course equips students with vital skills in model optimization, embedded AI deployment, runtime profiling, and hardware-software co-design, which are directly required for roles in system-on-chip development, neural processing unit design, semiconductor manufacturing, and intelligent edge-system engineering.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	2	-	-	-	-	-	2	3	2	2
CO2	3	3	3	2	3	-	-	-	-	-	2	3	3	2
CO3	3	2	3	2	3	-	-	-	1	-	2	3	3	3
CO4	3	3	3	3	3	-	-	1	1	-	2	3	3	2
CO5	3	3	3	3	3	1	1	1	1	1	3	3	3	3
Weighted Average	3.00	2.80	2.80	2.40	2.80	1.00	1.00	1.00	1.00	1.00	2.20	3.00	2.80	2.40

Course Code: U23EVV63
Course Title: SEMICONDUCTOR PROCESS INTEGRATION
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Semiconductor Manufacturing Technology, CMOS Integrated Circuits
SDG: 9

Course Overview

This course provides a comprehensive exploration of semiconductor process integration, bridging fundamental manufacturing modules with advanced CMOS technology flows. Students will analyze the interactions between front-end-of-line (FEOL) and back-end-of-line (BEOL) processes while addressing physical constraints and scaling challenges. The curriculum equips future engineers with the analytical skills necessary for optimizing device yield, managing process variability, and driving innovation in modern VLSI fabrication facilities.

Course Objectives

1. To analyze the interactions and compatibility constraints among various semiconductor manufacturing modules during the integration of CMOS technology flows.
2. To evaluate front-end-of-line, middle-of-line, and back-end-of-line integration schemes for advanced node architectures and interconnect systems.
3. To apply statistical process control methodologies and design of experiment techniques for managing process variability and optimizing manufacturing yield.

Unit I: PROCESS INTEGRATION FUNDAMENTALS **9 Hours**
Introduction to semiconductor process integration - Role of process integration in semiconductor manufacturing - Technology development cycle - Process-flow representation and integration sequence - Process modules and module interactions - Design rules and technology requirements - Thermal budget and thermal-cycle management - Contamination control and process compatibility - CMOS process integration challenges and technology scaling.
Active Learning Activity: Develop a simplified CMOS process-flow diagram and identify the interactions, compatibility constraints and thermal-budget requirements between major process modules.

Unit II: FRONT-END-OF-LINE PROCESS INTEGRATION **9 Hours**
FEOL integration requirements - Well formation and channel engineering - Isolation integration: LOCOS and STI - Gate-stack integration - High-k dielectric and metal-gate integration - Work-function engineering - Source/drain, LDD, halo and pocket engineering - Spacer, dopant activation and silicide integration - Contact formation, thermal budget and variability challenges.
Active Learning Activity: Compare planar CMOS FEOL integration schemes and identify the interaction between isolation, gate stack, source/drain engineering, annealing and contact formation.

Unit III: MOL AND BEOL PROCESS INTEGRATION **9 Hours**
Middle-of-Line integration concepts - Contact and local-interconnect formation - Contact resistance and contact engineering - Back-End-of-Line architecture - Interlayer dielectrics and

multilevel metallization - Aluminum and copper interconnect integration - Damascene and dual-damascene processes - Barrier, liner, low-k and ultra-low-k dielectric integration - CMP, interconnect scaling and reliability: RC delay, electromigration and TDDB.
Active Learning Activity: Analyze the effect of interconnect scaling and low-k dielectric integration on RC delay and major interconnect reliability mechanisms.

Unit IV: ADVANCED CMOS TECHNOLOGY INTEGRATION 9 Hours
Technology scaling and integration challenges - Strain engineering - Silicon-on-Insulator integration - FinFET process integration - High-k/metal-gate integration: gate-first and gate-last approaches - Gate-All-Around transistor integration - Nanosheet and selective-epitaxy integration - Advanced contacts, self-aligned processes and multiple-patterning concepts - 3D and monolithic 3D integration; beyond-planar CMOS trends.
Active Learning Activity: Compare the process-integration flows of planar CMOS, FinFET and GAA/nanosheet technologies using simplified cross-sectional representations.

Unit V: PROCESS CONTROL, VARIABILITY AND YIELD OPTIMIZATION 9 Hours
Process window and process capability - Sources of semiconductor process variability - Within-wafer and wafer-to-wafer variation - Critical-dimension, overlay and film-thickness variation - Statistical Process Control (SPC) - Process capability indices - Design of Experiments (DoE) for process optimization - Process monitoring, defectivity and inline metrology - Yield analysis, process-device correlation and yield learning.
Active Learning Activity: Perform a simple DoE or statistical analysis of process-parameter variation and evaluate its effect on device performance and manufacturing yield.

Course Outcomes

CO1: Apply semiconductor process-integration principles, process-module interactions and technology requirements to construct CMOS manufacturing flows. (K3)
CO2: Analyze FEOL integration strategies involving isolation, gate-stack, source/drain and contact formation in advanced CMOS technologies. (K4)
CO3: Analyze MOL and BEOL integration schemes, interconnect scaling and associated reliability mechanisms. (K4)
CO4: Compare process-integration approaches for planar CMOS, FinFET, GAA/nanosheet and 3D semiconductor technologies. (K4)
CO5: Evaluate process variability, statistical process control, design-of-experiments and yield-learning techniques for semiconductor manufacturing. (K5)

Resources

1. Text Books

1. Campbell, S. A. (2020). *The Science and Engineering of Microelectronic Fabrication* (4th ed.). Oxford University Press.

2. Xiao, H. (2019). *Introduction to Semiconductor Manufacturing Technology* (2nd ed.). SPIE Press.

3. May, G. S., & Sze, S. M. (2021). *Fundamentals of Semiconductor Fabrication* (3rd ed.). Wiley.

4. Plummer, J. D., Deal, M. D., & Griffin, P. B. (2022). *Silicon VLSI Technology: Fundamentals, Practice and Modeling* (2nd ed.). Pearson.
5. Franssila, S. (2023). *Introduction to Microfabrication* (3rd ed.). Wiley.

2. Reference Books

1. Colinge, J. P., & Greer, J. C. (2020). *Nanowire Transistors: Physics of Devices and Materials in One Dimension*. Cambridge University Press.
2. Doering, R., & Nishi, Y. (2019). *Handbook of Semiconductor Manufacturing Technology* (3rd ed.). CRC Press.
3. Baklanov, M. R., Green, M., & Maex, K. (2021). *Dielectric Films for Advanced Microelectronics*. Wiley.
4. Chen, M. (2022). *Advanced CMOS Process Integration: FinFET and GAA Technologies*. Springer.
5. Smith, L. (2023). *Semiconductor Process Integration, Variability and Yield Engineering*. McGraw-Hill.

3. E-Resources

1. NPTEL. (2022). *IC Technology* [Video course]. NPTEL. `https://nptel.ac.in/courses/117106093`
2. NPTEL. (2021). *VLSI Technology* [Video course]. NPTEL. `https://nptel.ac.in/courses/117106093`
3. MIT OpenCourseWare. (2020). *Microelectronic Devices and Circuits* [Course materials]. MIT. `https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/`
4. National Institute of Standards and Technology. (2023). *Semiconductor Metrology and Statistical Process Control Resources*. NIST. `https://www.nist.gov/semiconductor`
5. Coursera. (2022). *Semiconductor Processing and Advanced Device Integration*. Coursera. `https://www.coursera.org/learn/semiconductor-manufacturing`

Industrial Relevance

Semiconductor process integration is central to translating individual fabrication modules into manufacturable CMOS technologies. Modern semiconductor manufacturing requires coordinated control of FEOL, MOL and BEOL processes, thermal budgets, materials compatibility, interconnect reliability, process variability and yield. The course is particularly relevant to advanced CMOS technologies such as FinFET and GAA/nanosheet devices and to process-control and yield-engineering activities in global semiconductor fabrication facilities and commercial foundries.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	2	–	–	–	–	–	2	3	3	2
CO2	3	3	3	2	3	–	–	–	–	–	2	3	3	3
CO3	3	3	3	3	3	–	–	–	–	–	2	3	3	3
CO4	3	3	3	3	3	1	–	–	–	–	2	3	3	3
CO5	3	3	2	3	3	1	–	–	1	–	2	3	3	3
Weighted Average	3.00	3.00	2.60	2.60	2.80	1.00	–	–	1.00	–	2.00	3.00	3.00	2.80

Course Code: U23EVV64
Course Title: ADVANCED LITHOGRAPHY AND PROCESS TECHNOLOGIES
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Semiconductor Manufacturing Technology, CMOS Integrated Circuits
SDG: 9

Course Overview

This course provides advanced knowledge of semiconductor lithography and pattern-transfer technologies used in modern VLSI fabrication. It covers optical lithography, resolution enhancement, multiple-patterning techniques, extreme ultraviolet lithography, and next-generation nanoscale patterning methodologies. Furthermore, the curriculum emphasizes atomic-scale etching, deposition processes, metrology, and defectivity analysis to optimize manufacturing yields and ensure robust fabrication processes.

Course Objectives

1. Analyze the resolution limits, optical proximity effects, and enhancement techniques inherent in advanced optical lithography systems.
2. Evaluate multiple-patterning architectures, extreme ultraviolet lithography, and emerging nanoscale pattern-transfer technologies for advanced semiconductor manufacturing.
3. Assess atomic-scale etching, selective deposition processes, and rigorous lithography metrology to optimize process windows and maximize fabrication yield.

Unit I: Advanced Optical Lithography **9 Hours**
Evolution of semiconductor lithography and scaling - Diffraction, Rayleigh resolution and depth of focus - Numerical aperture and partial coherence - Photoresist characteristics and chemically amplified resists - Optical proximity effects - Resolution enhancement techniques - Off-axis illumination and phase-shift masks - Optical proximity correction and source-mask optimization - Immersion lithography and lithography process window.
Active Learning Activity: Analyze the effects of wavelength, numerical aperture, and process parameters on lithographic resolution and depth of focus using an open-source lithography simulation environment.

Unit II: Multiple Patterning and EUV Lithography **9 Hours**
Limitations of single-pattern optical lithography - Double-patterning and Litho-Etch-Litho-Etch processes - Self-Aligned Double Patterning - Self-Aligned Quadruple Patterning - Pattern decomposition and overlay requirements - EUV lithography fundamentals and radiation generation - EUV reflective optics and multilayer mirrors - EUV masks and photoresists - EUV stochastic effects and High-NA defectivity.
Active Learning Activity: Compare immersion multiple-patterning and EUV lithography in terms of resolution, overlay, process complexity, and defectivity through a comparative group evaluation.

Unit III: Next-Generation Patterning Technologies **9 Hours**
Electron-beam lithography fundamentals - Electron-beam interaction and proximity effects -

Mask writing and multi-beam lithography - Nanoimprint lithography - Thermal and UV nanoimprint techniques - Directed self-assembly and block-copolymer patterning - Maskless and laser-interference lithography - Focused-ion-beam patterning concepts - Comparison and applications of next-generation patterning technologies.
Active Learning Activity: Evaluate electron-beam, nanoimprint, and directed-self-assembly technologies based on resolution and throughput constraints using a structured process flow mapping exercise.

Unit IV: Atomic-Scale Pattern Transfer Technologies **9 Hours**
Pattern-transfer requirements for nanoscale fabrication - Plasma etching for nanoscale features - Anisotropic and selective etching - High-aspect-ratio and aspect-ratio-dependent etching - Atomic Layer Etching - Selective etching and pattern-collapse control - Atomic Layer Deposition and conformal deposition - Area-selective deposition and spacer-based patterning - Self-aligned processes and etch-deposition interactions.
Active Learning Activity: Develop a conceptual process sequence combining lithography, deposition, and etching for nanoscale pattern transfer and evaluate atomic-scale control mechanisms.

Unit V: Patterning Metrology and Process Optimization **9 Hours**
Critical-dimension metrology and characterization - Scatterometry and profile measurement - Overlay metrology and registration - Mask and defect inspection - Line-edge and line-width roughness - Pattern fidelity and resist-profile characterization - Process-window and exposure latitude analysis - Focus-exposure matrix and yield optimization - Computational lithography and lithography-aware design.
Active Learning Activity: Analyze a focus-exposure process-window matrix to determine suitable operating conditions and exposure latitude for an advanced lithography process using analytical modeling.

Course Outcomes

On successful completion of the course, students will be able to:

- CO1: Analyze diffraction, resolution limits and resolution-enhancement techniques in advanced optical lithography. (K4)
- CO2: Evaluate multiple-patterning and EUV lithography architectures with respect to resolution, overlay, stochastic effects and defectivity. (K5)
- CO3: Compare next-generation patterning technologies based on resolution, throughput, process complexity and application requirements. (K4)
- CO4: Analyze atomic-scale etching, selective deposition and self-aligned processes for high-fidelity nanoscale pattern transfer. (K4)
- CO5: Evaluate lithography metrology, process windows, defectivity and yield data for pattern-fidelity and process optimization. (K5)

Resources

1. Text Books

1. Levinson, H. J. (2021). *Principles of Lithography* (4th ed.). SPIE Press.
2. Mack, C. A. (2019). *Fundamental Principles of Optical Lithography: The Science of Microfabrication.* Wiley.

3. Suzuki, K., & Smith, B. W. (2020). *Microlithography: Science and Technology* (3rd ed.). CRC Press.

4. Plummer, J. D., Deal, M. D., & Griffin, P. B. (2020). *Silicon VLSI Technology: Fundamentals, Practice and Modeling* (2nd ed.). Pearson.

5. Wu, B., & Kumar, A. (2022). *Extreme Ultraviolet Lithography*. McGraw-Hill Education.

2. Reference Books

1. Wong, A. K. (2021). *Resolution Enhancement Techniques in Optical Lithography*. SPIE Press.

2. George, S. M. (2020). *Atomic Layer Etching and Deposition*. Springer.

3. Pease, R. F. (2019). *Next-Generation Nanofabrication and Pattern Transfer*. Cambridge University Press.

4. Sotomayor Torres, C. M. (2022). *Nanoimprint Lithography and Directed Self-Assembly*. Wiley-VCH.

5. Ruzic, D. N. (2023). *Plasma Processing for Semiconductor Fabrication*. IOP Publishing.

3. E-Resources

1. NPTEL. (2023). IC Fabrication and Advanced Lithography.
`https://nptel.ac.in/courses/108108113`

2. MIT OpenCourseWare. (2022). Nanoelectronics and Semiconductor Processing.
`https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/`

3. SPIE Digital Library. (2023). EUV Lithography and Process-Window Studies.
`https://www.spiedigitallibrary.org/`

4. IEEE Xplore. (2023). Multiple-Patterning and Computational Lithography.
`https://ieeexplore.ieee.org/`

5. Purdue University nanoHUB. (2021). Semiconductor Process and Lithography Simulation.
`https://nanohub.org/`

Industrial Relevance

Advanced lithography and pattern transfer are fundamental to modern semiconductor manufacturing. Extreme ultraviolet (EUV) lithography, self-aligned multiple patterning, atomic-layer etching, computational lithography, and precise metrology are critical for controlling nanometer-scale dimensions, edge placement, and defectivity in advanced CMOS technologies. This course bridges theoretical principles with current deployment practices, providing industry-aligned knowledge essential for careers in semiconductor foundries, electronic design automation (EDA) companies, lithography equipment manufacturing, and process integration development.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	2	–	–	–	1	–	2	3	3	2
CO2	3	3	3	3	3	–	–	1	1	–	2	3	3	3
CO3	3	3	2	2	2	–	–	–	1	–	2	3	3	2
CO4	3	3	3	3	3	–	1	1	1	–	2	3	3	3
CO5	3	3	3	3	3	1	1	1	2	1	2	3	3	3
Weighted Average	3.00	3.00	2.60	2.60	2.60	1.00	1.00	1.00	1.20	1.00	2.00	3.00	3.00	2.60

Course Code: U23EVV65
Course Title: SEMICONDUCTOR DEVICE MODELING using TCAD
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Electric Circuit and Electron Devices
SDG: 4, 9

Course Overview

This course introduces the fundamental principles, physical transport models, and numerical simulation methodologies essential for semiconductor device modeling. It provides a comprehensive analysis of MOS capacitors, nanoscale transistors, and multigate architectures to evaluate critical electrical characteristics. Furthermore, the curriculum emphasizes design-space exploration and parameter extraction workflows to optimize advanced VLSI technologies for industry-standard fabrication.

Course Objectives

1. Formulate the fundamental continuity equations and numerical boundary conditions required for precise semiconductor device electrostatics and transport modeling.
2. Analyze nanoscale device characteristics and physical mobility models to extract critical electrical parameters for advanced multi-gate architectures.
3. Evaluate design-space exploration methodologies and parametric sensitivity analysis to optimize device performance for modern fabrication nodes.

Unit I: Fundamentals of Device Modeling **9 Hours**
Introduction to semiconductor device modeling - Process simulation and device simulation workflows - Poisson equation and semiconductor electrostatics - Carrier continuity equations - Drift-diffusion carrier transport model - Carrier statistics and carrier concentrations - Generation and recombination mechanisms - Boundary conditions and numerical solution concepts - Mesh generation and refinement techniques.
Active Learning Activity: Develop a basic one-dimensional device electrostatic model and analyze the effect of mesh density variations on potential convergence accuracy using general-purpose numerical solvers.

Unit II: Physical Models and Device Simulation **9 Hours**
Device structure geometry and material definition - Doping profiles and electrode contact definition - Carrier mobility models - Shockley-Read-Hall and Auger recombination models - Bandgap narrowing and high-field effects - Impact ionization and carrier velocity saturation - Interface charges and surface mobility - Tunneling and advanced physical mechanisms - Physical-model selection and result calibration.
Active Learning Activity: Compare distinct mobility models systematically and analyze their direct influence on carrier concentration and internal electric field distributions through simulation visualization.

Unit III: MOS Device Modeling and Characterization **9 Hours**
MOS capacitor structure and electrostatic simulation - MOSFET structural parameters and numerical simulation - Transfer and output characteristics extraction - Threshold-voltage formulation and extraction - Subthreshold characteristics and subthreshold swing analysis - Transcon-

ductance and channel-length modulation effects - Short-channel effects and drain-induced barrier lowering - Leakage current and electric-field distribution profiling - Capacitance-voltage characteristics and parameter extraction.
Active Learning Activity: Simulate a fundamental MOSFET structure to mathematically extract and graph the threshold voltage, subthreshold swing, and peak transconductance from transfer characteristic data.

Unit IV: Nanoscale and Multigate Device Modeling **9 Hours**
MOSFET scaling limits and nanoscale device modeling - Two-dimensional and three-dimensional simulation concepts - Silicon-on-Insulator MOSFET modeling workflows - FinFET architecture and performance simulation - Gate-All-Around FET modeling principles - Nanosheet FET architecture and simulation dynamics - Multigate electrostatics and quantum-confinement effects - Advanced mobility interface and self-heating models - Extraction and comparison of vital on-off current ratios.
Active Learning Activity: Contrast FinFET and Gate-All-Around architectures by analyzing their simulated electrostatic potential contours to evaluate threshold voltage degradation and drain-induced barrier lowering.

Unit V: Device Optimization and Simulation Applications **9 Hours**
Parametric simulation and variable parameter sweeps - Sensitivity analysis and design-space exploration metrics - Geometry and doping concentration optimization - Device variability and statistical performance analysis - Device calibration and rigorous parameter extraction - Compact-model parameter extraction methodologies - Device-to-circuit interface and mixed-mode simulation - Optimization utilizing targeted electrical performance metrics - Introduction to photovoltaic device modeling frameworks.
Active Learning Activity: Execute a systematic parametric sweep of designated channel dimensions to identify an optimal operating point minimizing leakage while preserving drive current metrics.

Course Outcomes

CO1: Apply semiconductor electrostatics, carrier-transport equations, and mesh-generation techniques to formulate device-simulation workflows. (K3)
CO2: Analyze mobility, recombination, and tunneling models for accurate semiconductor device transport simulation. (K4)
CO3: Analyze MOS capacitor and MOSFET characteristics to extract critical electrical parameters and evaluate short-channel effects. (K4)
CO4: Analyze quantum-confinement, interface, and self-heating effects in nanoscale and multigate device architectures. (K4)
CO5: Evaluate numerical simulation results and sensitivity analysis to optimize semiconductor devices through design-space exploration. (K5)

Resources

1. Text Books

1. Sze, S. M., Li, Y., & Ng, K. K. (2021). Physics of Semiconductor Devices (4th ed.). Wiley.
2. Taur, Y., & Ning, T. H. (2022). Fundamentals of Modern VLSI Devices (3rd ed.). Cambridge University Press.
3. Selberherr, S. (2020). Analysis and Simulation of Semiconductor Devices. Springer.

4. Vasileska, D., Goodnick, S. M., & Klimeck, G. (2019). Computational Electronics: Semi-classical and Quantum Device Modeling and Simulation. CRC Press.

5. Dutton, R. W., & Yu, Z. (2023). Technology CAD: Computer Simulation of IC Processes and Devices. Springer.

2. Reference Books

1. Lundstrom, M. S. (2022). Fundamentals of Carrier Transport. Cambridge University Press.

2. Fonash, S. J. (2019). Solar Cell Device Physics. Academic Press.

3. Snowden, C. M. (2020). Introduction to Semiconductor Device Modelling. World Scientific.

4. Colinge, J. P. (2021). FinFETs and Other Multi-Gate Transistors. Springer.

5. Arora, N. (2023). MOSFET Modeling for VLSI Simulation: Theory and Practice. World Scientific.

3. E-Resources

1. NPTEL. (2023). Semiconductor Device Modeling [Video lectures]. `https://nptel.ac.in/courses/117106093`

2. nanoHUB. (2022). Semiconductor modeling and simulation resources [Tools]. `https://nanohub.org/groups/semiconductors`

3. MIT OpenCourseWare. (2021). Microelectronic Devices and Circuits [Course materials]. `https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/`

4. IEEE Xplore. (2023). IEEE Transactions on Electron Devices [Journals]. `https://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=16`

5. NPTEL. (2022). Advanced Semiconductor Devices [Video lectures]. `https://nptel.ac.in/courses/117106091`

Industrial Relevance

Device modeling is fundamentally critical to modern semiconductor technology development, enabling engineers to accurately predict device behavior, validate architectural changes, and optimize process parameters prior to physical fabrication. By mastering these simulation workflows, practitioners can significantly reduce the experimental development cycle for advanced CMOS technologies such as FinFET and Nanosheet architectures. Consequently, the analytical skills cultivated in this course are directly aligned with the highly specialized demands of global semiconductor foundries, process-development laboratories, and electronic design automation organizations, fostering the rapid deployment of next-generation VLSI platforms.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	3	-	-	-	-	-	2	3	2	2
CO2	3	3	2	3	3	-	-	-	1	-	2	3	3	2
CO3	3	3	3	3	3	-	-	1	1	-	2	3	3	3
CO4	3	3	3	3	3	1	-	1	1	-	2	3	3	3
CO5	3	3	3	3	3	1	1	1	1	1	3	3	3	3
Weighted Average	3.00	3.00	2.60	2.80	3.00	1.00	1.00	1.00	1.00	1.00	2.20	3.00	2.80	2.60

Course Code: U23EVV66
Course Title: SEMICONDUCTOR RELIABILITY AND YIELD ENGINEERING
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design, CMOS Integrated Circuits, Semiconductor Manufacturing Technology
SDG: 9

Course Overview

This course introduces the fundamental principles of semiconductor reliability and manufacturing yield engineering to systematically evaluate device lifetime and production quality. It covers essential reliability metrics, major physical degradation mechanisms, accelerated life-testing models, and statistical defect-density models to characterize complex semiconductor behavior under electrical and thermal stress. Emphasis is placed on understanding statistical manufacturing yield evaluation, reliability qualification methodologies, and yield enhancement strategies critically relevant to modern semiconductor technologies.

Course Objectives

1. Apply statistical reliability distributions and empirical acceleration models to mathematically characterize component failure behavior and estimate operational lifetime.
2. Analyze physical degradation mechanisms, defect-density distributions, and critical-area yield models to deeply evaluate semiconductor manufacturing limitations.
3. Evaluate sophisticated semiconductor product reliability qualification protocols, wafer-level screening techniques, and yield enhancement strategies for scalable industrial applications.

Unit I: SEMICONDUCTOR RELIABILITY FUNDAMENTALS 9 Hours
Reliability, quality and availability concepts – Failure rate and hazard rate – Mean Time To Failure (MTTF) and Mean Time Between Failures (MTBF) – Bathtub curve and reliability life-cycle phases – Reliability and cumulative failure functions – Exponential distribution – Normal distribution – Lognormal distribution – Weibull distribution – Intrinsic and extrinsic failure mechanisms – Reliability challenges in scaled semiconductor technologies.
Active Learning Activity: Generate a sample failure dataset and use statistical analysis to estimate failure characteristics, hazard rate and mean time to failure.

Unit II: DEVICE AND INTERCONNECT RELIABILITY 9 Hours
Semiconductor device failure mechanisms – Gate-dielectric reliability – Time-Dependent Dielectric Breakdown (TDDB) – Bias Temperature Instability (NBTI and PBTI) – Hot Carrier Injection (HCI) – Junction leakage and device degradation – Electromigration – Interconnect reliability and thermal effects – Self-heating – Reliability challenges due to technology scaling.
Active Learning Activity: Analyze the effect of current density and temperature on electromigration and identify the major factors influencing interconnect reliability using generic open-source circuit simulation tools.

Unit III: RELIABILITY TESTING AND LIFETIME PREDICTION 9 Hours
Accelerated Life Testing principles – Temperature, voltage and current acceleration – Arrhenius acceleration model – Eyring acceleration model – Voltage acceleration concepts – Black's

equation for electromigration – Weibull failure-data analysis – Lifetime extrapolation – High Temperature Operating Life (HTOL) – Highly Accelerated Stress Test (HAST) – Reliability prediction.
Active Learning Activity: Apply the Arrhenius model and Weibull analysis to accelerated-stress data and estimate expected operational lifetime under normal conditions.

Unit IV: SEMICONDUCTOR YIELD MODELING AND ANALYSIS 9 Hours
Semiconductor manufacturing yield concepts – Wafer yield and die yield – Functional and parametric yield – Defect density and defect classification – Random and systematic defects – Critical-area analysis – Defect-limited yield – Poisson yield model – Murphy yield model – Negative-binomial yield model – Process variation – Wafer maps and yield signatures.
Active Learning Activity: Analyze synthetic wafer-inspection data to identify defect patterns, construct wafer maps and compare statistical yield predictions.

Unit V: RELIABILITY QUALIFICATION AND YIELD ENHANCEMENT 9 Hours
Reliability qualification methodology – Product qualification and reliability monitoring – Reliability screening – Burn-in and early-life failure concepts – Reliability sampling and qualification planning – Wafer-level and package-level reliability – Yield learning and yield ramp – Yield-loss diagnosis – Pareto analysis – Manufacturing excursion analysis – Design for Reliability (DfR) – Reliability and yield improvement strategies – Industrial case studies.
Active Learning Activity: Analyze a representative manufacturing yield excursion using reliability and yield data, identify major failure contributors and propose suitable defect-reduction or reliability-improvement actions.

Course Outcomes

1. Apply statistical reliability distributions and reliability metrics to characterize semiconductor failure behavior and lifetime. (K3)
2. Analyze major physical and electrical degradation mechanisms in semiconductor devices and interconnects under electrical and thermal stress. (K4)
3. Analyze accelerated life-test data and reliability models to estimate semiconductor device and interconnect lifetime. (K4)
4. Analyze defect-density, critical-area and statistical yield models to evaluate semiconductor manufacturing yield and defect patterns. (K4)
5. Evaluate reliability qualification and yield-enhancement strategies to improve semiconductor product quality and manufacturing yield. (K5)

Resources

1. Text Books

1. McPherson, J. W. (2022). Reliability Physics and Engineering: Time-to-Failure Modeling (3rd ed.). Springer.
2. Birolini, A. (2021). Reliability Engineering: Theory and Practice (9th ed.). Springer.
3. Ohring, M., & Kasprzak, L. (2020). Reliability and Failure of Electronic Materials and Devices (3rd ed.). Academic Press.

4. May, G. S., & Spanos, C. J. (2023). Fundamentals of Semiconductor Manufacturing and Process Control (2nd ed.). Wiley-IEEE Press.

5. Bernstein, J. B., & Gurfinkel, M. (2019). Microelectronic Failure Analysis and Reliability Engineering. CRC Press.

2. Reference Books

1. Strong, A. W., et al. (2022). Reliability Wearout Mechanisms in Advanced CMOS Technologies. IEEE Press.

2. Amerasekera, E. A., & Najm, F. N. (2021). Failure Mechanisms in Semiconductor Devices (2nd ed.). Wiley.

3. Pecht, M. (2020). Product Reliability, Maintainability, and Supportability Handbook (3rd ed.). CRC Press.

4. Schroder, D. K. (2019). Semiconductor Material and Device Characterization (4th ed.). Wiley.

5. Sharma, A. (2023). Advanced Semiconductor Manufacturing Reliability and Verification. Cambridge University Press.

3. E-Resources

1. NPTEL. (2023). Reliability Engineering and Quality Control. [Note: Statistical Models]. `https://nptel.ac.in/courses/112106143`

2. NPTEL. (2023). VLSI Technology and Semiconductor Process Integration. [Note: Fabrication Processes].
   `https://nptel.ac.in/courses/117106093`

3. MIT OpenCourseWare. (2022). Microelectronic Device Reliability. [Note: Failure Mechanisms].
   `https://ocw.mit.edu/courses/electrical-engineering-and-computer-science`

4. IEEE Reliability Society. (2023). Educational Resources and Tutorials. [Note: Industry Standards].
   `https://rs.ieee.org/education`

5. NIST. (2023). Engineering Statistics Handbook: Reliability Statistics. [Note: Data Analysis].
   `https://www.itl.nist.gov/div898/handbook/apr/apr.htm`

Industrial Relevance

Semiconductor reliability and yield engineering are essential for ensuring product lifetime, manufacturing quality, and production yield in the modern electronics industry. This course provides critical knowledge of major CMOS degradation mechanisms, accelerated reliability testing, statistical lifetime prediction, and defect-density modeling that are fundamental to industrial fabrication processes. By mastering yield analysis and reliability qualification, engineers are directly equipped to lead Design for Reliability (DfR) activities, optimize manufacturing excursions, and deploy robust semiconductor solutions that meet rigorous global infrastructure standards, driving sustainable technological innovation worldwide.

CO-PO-PSO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	-	1	-	-	-	-	-	-	1	1	2	1
CO2	3	3	2	2	-	-	-	-	-	-	1	2	3	2
CO3	3	3	2	3	2	-	-	-	-	-	1	2	2	2
CO4	3	3	2	3	2	-	-	-	-	-	1	2	3	2
CO5	3	3	3	3	2	2	1	-	-	-	2	2	3	3
Weighted Average	3.00	2.80	2.25	2.40	2.00	2.00	1.00	-	-	-	1.20	1.80	2.60	2.00

Course Code: U23EVV67
Course Title: ADVANCED SEMICONDUCTOR PACKAGING
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisite: Semiconductor Manufacturing Technology
SDG: 9 (Industry, Innovation and Infrastructure)

Course Overview

This course provides an in-depth understanding of advanced semiconductor packaging technologies utilized for high-density system integration. It explores critical concepts including wafer-level integration, through-silicon vias, hybrid bonding, and thermal management architectures essential for modern heterogeneous systems. Furthermore, the curriculum emphasizes the evaluation of electrical integrity, thermo-mechanical stress, and reliability mechanisms to prepare students for real-world hardware deployment challenges.

Course Objectives

1. Analyze wafer-level, fan-out, and fine-pitch semiconductor packaging technologies to design high-density integration architectures.
2. Evaluate the electrical, thermal, and thermo-mechanical integrity of 2.5D and 3D heterogeneous integration systems to ensure robust performance.
3. Assess package reliability, qualification methodologies, and failure mechanisms to optimize emerging semiconductor packaging solutions.

Unit I: Wafer-Level and Fan-Out Packaging **9 Hours**
Evolution of advanced semiconductor packaging - Wafer-Level Packaging and Fan-In WLP - Fan-Out Wafer-Level Packaging - Redistribution Layer architectures - Wafer bumping and fine-pitch interconnections - Copper pillar and microbump technologies - Wafer thinning and back-grinding - Temporary bonding, debonding and embedded-die packaging - Panel-Level Packaging, Through-Mold Via and advanced substrates.
Active Learning Activity: Compare Fan-In and Fan-Out WLP architectures and analyze their redistribution-layer routing, interconnection density and package-integration advantages.

Unit II: TSV and 2.5D Integration **9 Hours**
Through-Silicon Via technology fundamentals - Via-first, via-middle and via-last approaches - TSV formation and dielectric isolation - Barrier, seed and TSV filling technologies - Wafer thinning and backside processing - Silicon, organic and glass interposers - 2.5D integration and die-to-interposer interconnection - Microbump and RDL-interposer technologies - High Bandwidth Memory integration and 2.5D design challenges.
Active Learning Activity: Analyze the electrical parasitics of a high-aspect-ratio TSV and study the effect of TSV dimensions and materials on resistance and capacitance.

Unit III: 3D and Heterogeneous Integration **9 Hours**
3D integrated-circuit integration concepts - Die-to-die, die-to-wafer and wafer-to-wafer stacking - Face-to-face and face-to-back integration - Hybrid bonding technology - Copper-to-copper direct bonding - Bond alignment and interface requirements - Heterogeneous integration of logic, memory, RF, sensors and photonics - System-in-Package and chiplet-based architectures - Die-to-die interconnects and heterogeneous-system design challenges.

Active Learning Activity: Develop a system-level partitioning of a monolithic system-on-chip into multiple chiplets and analyze the resulting die-to-die interconnection requirements.

Unit IV: Electrical, Thermal and Thermo-Mechanical Integrity **9 Hours**
Electrical parasitics in advanced package interconnects - Signal integrity in interposers and chiplet systems - Power integrity and power-delivery networks - Thermal resistance in stacked devices - Hotspot formation and heat spreading - Thermal Interface Materials - Advanced package cooling technologies - CTE mismatch, thermo-mechanical stress and package warpage - TSV, microbump and bonding-interface stress and coupled multi-physics effects.
Active Learning Activity: Analyze a 3D stacked memory-logic structure and identify thermal hotspots, heat-flow paths and critical thermo-mechanical stress regions.

Unit V: Package Reliability and Emerging Technologies **9 Hours**
Reliability of advanced semiconductor packages - Microbump and solder-joint fatigue - Interfacial delamination and die cracking - TSV reliability and package-interconnect degradation - Electromigration and thermal-cycling reliability - Moisture-induced and warpage-related failures - Package-level qualification and failure-analysis concepts - Chiplet packaging, high bandwidth memory and glass-substrate technologies - Co-packaged optics, advanced thermal solutions and emerging heterogeneous integration.
Active Learning Activity: Analyze a package-reliability failure case and identify the root cause of solder-joint fatigue or electromigration using reliability data.

Course Outcomes

On successful completion of the course, students will be able to:

CO1: Apply wafer-level, fan-out, redistribution-layer and fine-pitch interconnection concepts to advanced semiconductor packaging architectures. (K3)

CO2: Analyze TSV, interposer, microbump and 2.5D integration architectures for high-bandwidth semiconductor systems. (K4)

CO3: Analyze 3D stacking, hybrid bonding and chiplet-based heterogeneous integration architectures. (K4)

CO4: Analyze electrical, power, thermal and thermo-mechanical integrity in advanced multi-die packages. (K4)

CO5: Evaluate package reliability, qualification methods and emerging heterogeneous-integration technologies for advanced semiconductor systems. (K5)

Resources

1. Text Books

1. Lau, J. H. (2022). *Heterogeneous Integration*. Springer.
2. Lau, J. H. (2021). *Fan-Out Wafer-Level Packaging*. Springer.
3. Chen, A., & Lo, R. H.-Y. (2020). *Semiconductor Packaging: Materials Interaction and Reliability*. CRC Press.
4. Lau, J. H. (2023). *State-of-the-Art and Trends in Advanced Packaging*. Springer.
5. Tummala, R. R., & Swaminathan, M. (2019). *Introduction to System-on-Package (SOP): Miniaturization of the Entire System*. McGraw-Hill Education.

2. Reference Books

1. Lau, J. H. (2020). *3D IC Integration and Packaging*. Springer.
2. Tummala, R. R. (2019). *Fundamentals of Microsystems Packaging*. McGraw-Hill Education.
3. Lau, J. H. (2021). *Through-Silicon Vias for 3D Integration*. McGraw-Hill.
4. Harper, C. A. (2020). *Electronic Packaging and Interconnection Handbook*. McGraw-Hill.
5. Pecht, M., & Das, D. (2022). *Thermo-mechanical Reliability of Advanced Semiconductor Packages*. Springer.

3. E-Resources

1. NPTEL - Electronic Packaging and Manufacturing (Note: Video Lectures and Materials). `https://nptel.ac.in/courses/108108167`
2. NPTEL - IC Packaging Technology (Note: Advanced Interconnection Modules). `https://nptel.ac.in/courses/108104168`
3. IEEE Electronics Packaging Society - Heterogeneous Integration resources (Note: Technical Articles and Guidelines). `https://eps.ieee.org/technology/heterogeneous-integration.html`
4. MIT OpenCourseWare - Microelectronics and packaging resources (Note: Lecture Notes). `https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/`
5. NPTEL - Advanced VLSI Interconnection (Note: Semiconductor Packaging Simulation). `https://nptel.ac.in/courses/117101105`

Industrial Relevance

Advanced semiconductor packaging is increasingly vital as conventional monolithic system-on-chip scaling faces physical, thermal, and reticle-size limitations. Technologies such as 2.5D interposers, 3D stacking, microbumps, hybrid bonding, and chiplet architectures enable the high-bandwidth and energy-efficient systems required for artificial intelligence accelerators, high-performance computing, automotive electronics, and telecommunications. By developing core competencies in power integrity, thermal management, thermo-mechanical analysis, and package reliability, this course ensures students are equipped with the specialized engineering skills demanded by the global semiconductor manufacturing and fabrication industry.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	-	2	1	-	-	1	-	2	3	3	2
CO2	3	3	3	2	3	-	-	-	1	-	2	3	3	2
CO3	3	3	3	2	3	1	-	1	1	-	2	3	3	3
CO4	3	3	3	3	3	-	-	-	1	-	2	3	3	2
CO5	3	3	3	3	3	1	1	1	1	1	3	3	3	3
Weighted Average	3.00	2.80	2.80	2.50	2.80	1.00	1.00	1.00	1.00	1.00	2.20	3.00	3.00	2.40

Course Code: U23EVV68
Course Title: Semiconductor Product Engineering and Failure Analysis
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisite: Digital System Design
SDG: 9

Course Overview

This course introduces semiconductor product engineering and failure-analysis methodologies used to bridge integrated circuit design, silicon manufacturing, production testing, and product qualification. It emphasizes the systematic diagnosis of die, interconnect, package, and production-test failures alongside the formulation of structured feedback to design, process, test, and packaging teams. Students will gain practical expertise in yield-signature analysis, physical failure localization, root-cause analysis, and standardized corrective-action methodologies essential for high-volume manufacturing environments.

Course Objectives

1. To analyze wafer-sort, final-test, and parametric test data to identify yield signatures and evaluate semiconductor production qualification processes.
2. To apply electrical, optical, thermal, and physical localization techniques for isolating and verifying complex semiconductor functional failures.
3. To formulate silicon-debug and corrective-action methodologies for resolving physical failure mechanisms and improving overall semiconductor yield.

Unit I: Semiconductor Product Engineering **9 Hours**
Semiconductor product-engineering lifecycle - Product introduction and technology transfer - Datasheet specifications and electrical requirements - Silicon characterization methodologies - Process-Voltage-Temperature characterization - Production test-limit development - Guard banding and test-limit optimization - Product corners and qualification limits - Production ramp and product-engineering functions.
Active Learning Activity: Analyze a representative PVT characterization dataset to determine suitable test limits, guard bands, and qualification corners.
Unit II: Product Test and Data Analysis **9 Hours**
Wafer probing and wafer-sort methodology - Final test and production test flow - Parametric and functional testing - Test limits, datalogs and test bins - Binning and bin-yield analysis - Shmoo plots and operating-window analysis - Wafer maps and spatial yield patterns - Statistical test-data analysis and outlier detection - Yield signatures, test correlation and production monitoring.
Active Learning Activity: Generate Shmoo plots and wafer-map representations from a representative test dataset to identify abnormal yield patterns.
Unit III: Failure Localization and Analysis Techniques **9 Hours**
Failure-analysis methodology and failure verification - Electrical characterization and fault isolation - Optical microscopy and emission microscopy - Thermal localization techniques - OBIRCH and electrical fault-localization concepts - X-ray inspection and Scanning Acoustic Microscopy - SEM-based physical analysis - FIB and TEM-based analysis concepts - Sample preparation: decapsulation, cross-sectioning and delayering.

Active Learning Activity: Select appropriate non-destructive and destructive failure-localization techniques for representative open-circuit and short-circuit failure cases.

Unit IV: Physical Failure Analysis and Root Cause **9 Hours**

Die-level failure mechanisms - Interconnect and contact failures - Open and short failure signatures - Gate-oxide and junction failure mechanisms - Contamination-related failure mechanisms - ESD and EOS failure signatures - Package-related and solder/interconnect failures - Design-process-package-test correlation - Root-cause analysis using fault trees and 5-Why methodology.
Active Learning Activity: Construct a fault tree and perform a 5-Why analysis for a representative ESD/EOS or interconnect-failure scenario.

Unit V: Silicon Debug and Corrective Action **9 Hours**

Silicon debug methodology - Classification of design, process and test failures - Yield-loss diagnosis - Wafer-map and lot-level correlation - Test-limit optimization - Corrective and Preventive Action methodology - 8D problem-solving methodology - Failure-analysis reporting and feedback - Product improvement and semiconductor product-engineering case studies.
Active Learning Activity: Prepare an 8D Corrective and Preventive Action report for a simulated multi-lot yield-loss problem and identify feedback actions for design, process, test, and packaging teams.

Course Outcomes (COs)

On successful completion of the course, students will be able to:

- CO1: Apply semiconductor product-engineering principles, PVT characterization, and guard-banding techniques to establish production test limits. (K3)
- CO2: Analyze wafer-sort, final-test, and parametric test data using statistical analysis, Shmoo plots, and wafer maps to identify product-yield signatures. (K4)
- CO3: Analyze electrical, optical, thermal, and physical failure-localization techniques to isolate semiconductor functional failures. (K4)
- CO4: Analyze physical failure mechanisms, ESD/EOS signatures, and interconnect anomalies using structured root-cause analysis techniques. (K4)
- CO5: Evaluate silicon-debug and corrective-action methodologies to identify design, process, test, and packaging contributors to semiconductor yield loss. (K5)

Resources

1. Text Books

1. Schroder, D. K. (2021). *Semiconductor Material and Device Characterization* (4th ed.). IEEE Press.
2. Ross, R. J. (2022). *Microelectronic Failure Analysis Desk Reference* (7th ed.). ASM International.
3. Hnatek, E. R. (2020). *Integrated Circuit Quality and Reliability* (3rd ed.). CRC Press.
4. Kitchin, J. (2021). *Applied Reliability for Electronic Systems.* Artech House.
5. Sharma, A. (2023). *Semiconductor Product Engineering and Yield Optimization.* Springer.

2. Reference Books

1. Vaisband, B., & Friedman, E. G. (2022). *On-Chip Power Delivery and Management*. Springer.
2. Doering, R., & Nishi, Y. (2020). *Handbook of Semiconductor Manufacturing Technology* (3rd ed.). CRC Press.
3. Pecht, M. G. (2021). *Prognostics and Health Management of Electronics*. Wiley-IEEE Press.
4. O'Connor, P., & Kleyner, A. (2020). *Practical Reliability Engineering* (6th ed.). Wiley.
5. Kasap, S. O. (2023). *Principles of Electronic Materials and Devices* (4th ed.). McGraw-Hill Education.

3. E-Resources

1. NPTEL. (2022). IC Manufacturing and Yield Engineering. Note: Wafer sort and final test flow.
   `https://nptel.ac.in`
2. IEEE Xplore. (2023). Semiconductor failure localization and analysis. Note: Advanced fault isolation methods.
   `https://ieeexplore.ieee.org`
3. NIST. (2021). Semiconductor characterization and testing resources. Note: PVT characterization methodologies.
   `https://www.nist.gov`
4. NPTEL. (2023). Quality Control and Reliability Engineering. Note: Root-cause and statistical yield analysis.
   `https://nptel.ac.in`
5. Semiconductor Research Corporation. (2020). Physical failure analysis and ESD/EOS. Note: Failure analysis reporting.
   `https://www.src.org`

Industrial Relevance

This course is directly relevant to semiconductor product-engineering, production-test, failure-analysis, and yield-engineering functions in high-volume semiconductor manufacturing, fabless integrated circuit organizations, and semiconductor testing laboratories. Its rigorous emphasis on wafer sort, operating-window analysis, wafer maps, fault isolation, physical failure analysis, root-cause analysis, and systematic problem-solving methodology provides a practical bridge between design, foundry process, test, packaging, and product engineering. By integrating active yield-data analysis and failure localization, graduates are equipped to accelerate technology nodes and resolve complex manufacturing anomalies in modern semiconductor facilities.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	2	-	-	-	-	-	2	3	3	2
CO2	3	3	2	3	3	-	-	1	1	-	2	3	3	3
CO3	3	3	2	3	3	-	-	-	1	-	2	3	3	2
CO4	3	3	2	3	2	-	-	1	1	-	2	3	3	3
CO5	3	3	3	3	3	1	1	1	1	1	3	3	3	3
Weighted Average	3.00	3.00	2.20	2.80	2.60	1.00	1.00	1.00	1.00	1.00	2.20	3.00	3.00	2.60

Course Code: U23EVV69
Course Title: REAL-TIME EMBEDDED SOFTWARE AND SYSTEMS
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisite: Embedded Systems Architecture and Design
SDG: SDG 9

Course Overview

This course introduces real-time embedded systems with emphasis on deterministic timing, task scheduling, synchronization, real-time operating-system services, worst-case execution-time analysis, performance profiling, and power-aware embedded-system design. Applications span across automotive, industrial, robotics, and Internet of Things domains where predictable execution and reliability are paramount. Through theoretical foundations and practical design paradigms, students learn to architect robust firmware that satisfies strict temporal and resource constraints.

Course Objectives

1. Understand real-time task models, timing constraints, and fundamental real-time kernel mechanisms.
2. Analyze fixed- and dynamic-priority scheduling algorithms, schedulability conditions, and response-time verification.
3. Evaluate inter-task communication, synchronization mechanisms, and deadlock-resolution protocols for reliable real-time execution.

Unit I: Real-Time Embedded System Fundamentals **9 Hours**
Introduction to Real-Time Embedded Systems - Hard, Firm and Soft Real-Time Systems - Timing Constraints and Deadlines - Response-Time Analysis - Jitter and Timing Variations - Real-Time Task Characterization - Periodic Task Models - Aperiodic and Sporadic Task Models - Fundamental Real-Time Kernel Mechanisms.
Active Learning Activity: Analyze timing diagrams of automotive electronic-control tasks and classify them as hard, firm or soft real-time tasks based on deadline and failure constraints.
Unit II: Real-Time Scheduling **9 Hours**
Real-Time Task States and Scheduling Models - Preemptive and Non-Preemptive Scheduling - Static and Dynamic Priority Assignment - Rate Monotonic Scheduling - Deadline Monotonic Scheduling - Earliest Deadline First Scheduling - Processor Utilization and Utilization Bounds - Schedulability Analysis - Response-Time Verification.
Active Learning Activity: Implement and compare Rate Monotonic and Earliest Deadline First scheduling for synthetic task sets and evaluate processor utilization and deadline misses.
Unit III: Inter-Task Communication and Synchronization **9 Hours**
Inter-Task Communication Fundamentals - Critical Sections and Mutual Exclusion - Race Conditions and Their Prevention - Semaphores - Message Queues and Mailboxes - Event Flags and Event Synchronization - Deadlock Conditions and Prevention - Priority Inversion - Priority Inheritance and Priority Ceiling Protocols.
Active Learning Activity: Create a simulated priority-inversion scenario and resolve it using priority inheritance and priority-ceiling synchronization mechanisms.

Unit IV: Real-Time Operating Systems **9 Hours**

Real-Time Operating-System Architecture - RTOS Kernel Services - Task Creation, Scheduling and Deletion - Context Switching and Latency - Interrupt Service Routine Handling - Real-Time Timer Management - Dynamic Memory Management - RTOS Inter-Task Communication Services - RTOS APIs and Open-Source RTOS Application Development.

Active Learning Activity: Develop a multitasking sensor-monitoring application using an open-source real-time kernel and configure tasks, timers, communication services and stack allocation.

Unit V: Real-Time Embedded System Design **9 Hours**

RTOS-Based Embedded Application Architecture - Hardware-Software Interface and Device Drivers - Real-Time Data Acquisition Pipelines - Timing Measurement and Execution-Time Analysis - Worst-Case Execution-Time Analysis - Performance Profiling and Optimization - Real-Time System Debugging - Power-Aware Real-Time System Design - Automotive, Industrial, Robotics and IoT Applications.

Active Learning Activity: Analyze a real-time industrial robotic-control application and estimate WCET for sensor-actuator control tasks while considering timing, thermal and energy constraints.

Course Outcomes

CO1. Apply real-time task models, timing constraints and kernel concepts to characterize real-time embedded systems. (K3)

CO2. Analyze fixed- and dynamic-priority scheduling algorithms using utilization bounds, schedulability tests and response-time analysis. (K4)

CO3. Analyze inter-task communication and synchronization mechanisms to resolve race conditions, deadlocks and priority inversion. (K4)

CO4. Configure RTOS task management, interrupt handling, timer services, memory management and communication APIs for embedded applications. (K3)

CO5. Evaluate worst-case execution time, performance profiling and power-aware techniques for real-time embedded applications. (K5)

Resources

1. Text Books

1. Laplante, P. A., & Ovaska, S. J. (2020). *Real-Time Systems Design and Analysis: Tools for the Practitioner* (5th ed.). IEEE Press/Wiley.

2. Noergaard, T. (2020). *Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers* (2nd ed.). Newnes.

3. Marwedel, P. (2021). *Embedded System Design: Embedded Systems Foundations of Cyber-Physical Systems* (3rd ed.). Springer.

4. Krishna, C. M., & Shin, K. G. (2022). *Real-Time Systems* (2nd ed.). McGraw-Hill Education.

5. Vahid, F., & Givargis, T. (2020). *Embedded System Design: A Unified Hardware/Software Introduction* (3rd ed.). Wiley.

2. Reference Books

1. Buttazzo, G. C. (2019). *Hard Real-Time Computing Systems: Predictable Scheduling Algorithms and Applications* (4th ed.). Springer.
2. Cottet, F., Delacroix, J., Kaiser, C., & Mammeri, Z. (2019). *Scheduling in Real-Time Systems*. Wiley.
3. Lee, E. A., & Seshia, S. A. (2020). *Introduction to Embedded Systems: A Cyber-Physical Systems Approach*. MIT Press.
4. Cooling, J. (2020). *Real-Time Operating Systems: Book 1 – The Theory*. SAP Publishing.
5. Valvano, J. W. (2021). *Embedded Systems: Real-Time Operating Systems for ARM Cortex-M Microcontrollers*. CreateSpace.

3. E-Resources

1. NPTEL. *Real-Time Systems Scheduling and Synchronization*. Note: Focuses on scheduling paradigms and semaphore management.
   `https://nptel.ac.in/courses/106105172`
2. NPTEL. *Embedded Systems Design and RTOS Architecture*. Note: Covers real-time operating system internals and peripheral interfacing.
   `https://nptel.ac.in/courses/108102045`
3. MIT OpenCourseWare. *Cyber-Physical Systems and Real-Time Computing*. Note: Advanced studies on timing analysis and verification.
   `https://ocw.mit.edu/courses/res-6-007-signals-and-systems-spring-2011/`
4. IEEE Xplore Digital Library. *Real-Time Kernel Implementation and Schedulability Analysis*. Note: Research collection on preemptive scheduling kernels.
   `https://ieeexplore.ieee.org/`
5. ACM Digital Library. *Worst-Case Execution Time and Power-Aware Real-Time Systems*. Note: Papers on energy-efficient embedded scheduling.
   `https://dl.acm.org/`

Industrial Relevance

Real-time embedded systems are fundamental to automotive electronics, industrial automation, robotics, IoT, and SoC-based embedded platforms. Deterministic scheduling, synchronization, WCET analysis, interrupt-latency management, and power-aware design are critically important for systems operating under strict timing and energy constraints. The course provides essential preparation for real-time firmware development, RTOS-based embedded applications, and hardware-software co-design practices prevalent in modern semiconductor and embedded product industries.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	2	–	–	–	–	–	2	3	2	2
CO2	3	3	3	2	3	–	–	–	–	–	2	3	2	2
CO3	3	3	3	3	3	–	–	1	–	–	2	3	3	2
CO4	3	2	3	2	3	–	–	1	1	–	2	3	3	3
CO5	3	3	3	3	3	1	–	1	1	1	2	3	3	3
Weighted Average	3.00	2.80	2.80	2.40	2.80	1.00	–	1.00	1.00	1.00	2.00	3.00	2.60	2.40

Course Code: U23EVV70
Course Title: EMBEDDED LINUX AND DEVICE DRIVERS
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design, Computer Architecture and On-Chip Communication
SDG: 9

Course Overview

This course introduces the architecture and system-level programming methodologies required to develop, configure, and deploy customized operating systems on embedded hardware platforms. It provides a comprehensive understanding of system boot sequences, kernel compilation, device tree integration, and root filesystem construction. Furthermore, the curriculum emphasizes the practical development of character drivers, peripheral frameworks, and power management techniques essential for reliable System-on-Chip hardware-software integration.

Course Objectives

1. To configure and construct customized embedded operating system images by integrating bootloaders, kernels, device trees, and root filesystems using industry-standard build frameworks.
2. To develop and analyze loadable kernel modules, character device drivers, and platform drivers for seamless user-space and kernel-space interaction.
3. To implement advanced driver techniques including synchronization, direct memory access, and power management for reliable peripheral interfacing in complex embedded environments.

Unit I: EMBEDDED LINUX SYSTEM ARCHITECTURE **9 Hours**
Embedded Linux architecture and system components - Linux kernel and user-space architecture - Embedded Linux boot sequence - Bootloader concepts and boot stages - Linux kernel configuration - Linux kernel compilation and deployment - Root filesystem architecture - Cross-development environment and toolchain - Kernel command line and embedded Linux system initialization.
Active Learning Activity: Trace an embedded system boot sequence from the bootloader to initialization using a generic system simulator to identify the role of the kernel and root filesystem.
Unit II: EMBEDDED LINUX BUILD AND CONFIGURATION **9 Hours**
Linux kernel source organization and configuration - Cross-compilation and target deployment - Root filesystem creation - BusyBox and minimal Embedded Linux systems - Buildroot architecture and workflow - Yocto Project architecture and concepts - Packages, recipes and software integration - Board configuration and Embedded Linux image components - Bootloader, kernel, Device Tree and root filesystem integration.
Active Learning Activity: Configure a minimal system image using an open-source build framework and analyze the memory footprint of its kernel and application components.
Unit III: LINUX DEVICE DRIVER ARCHITECTURE **9 Hours**
Linux kernel modules and loadable-module architecture - Module loading, unloading and initialization - Linux kernel APIs and driver interfaces - Character device-driver architecture - Major

and minor device numbers - Device registration and file operations - User-space and kernel-space interaction - ioctl, sysfs and procfs interfaces - Kernel memory allocation and driver error handling.
Active Learning Activity: Develop a basic loadable character-device driver and demonstrate data exchange between a user-space application and a kernel-space driver using an open-source hardware emulator.

Unit IV: PLATFORM AND PERIPHERAL DRIVERS **9 Hours**

Linux device model - Platform devices and platform drivers - Device Tree fundamentals - Device Tree Source and hardware bindings - Driver probing and device matching - Memory-mapped I/O and register access - Interrupt handling in Linux device drivers - GPIO, I²C and SPI driver frameworks - UART, DMA and pinctrl concepts.
Active Learning Activity: Analyze a hardware description file for a custom peripheral and trace the sequence from hardware description to platform-device creation and driver probing.

Unit V: ADVANCED DRIVER DEVELOPMENT AND DEBUGGING 9 Hours

Synchronization in Linux device drivers - Spinlocks, mutexes and synchronization mechanisms - Completions and wait queues - Workqueues and deferred execution - Kernel timers - Memory mapping and DMA concepts - Power management in device drivers - Driver debugging, printk, dynamic debug and kernel logs - Kernel tracing, driver testing and development workflow.
Active Learning Activity: Analyze a driver synchronization problem involving concurrent access to shared kernel resources and implement appropriate locking and testing techniques within a simulated environment.

Course Outcomes

CO1: Apply Embedded Linux architecture, cross-compilation and bootloader concepts to configure and deploy Linux on an embedded SoC platform. (K3)
CO2: Construct a customized Embedded Linux image by integrating the bootloader, kernel, Device Tree and root filesystem using appropriate build frameworks. (K3)
CO3: Analyze Linux kernel modules and character-device-driver interfaces using kernel APIs, device registration and user-space communication mechanisms. (K4)
CO4: Analyze platform-driver architecture, Device Tree bindings, memory-mapped I/O, interrupts and peripheral frameworks for SoC-based embedded systems. (K4)
CO5: Evaluate synchronization, memory-management, DMA, power-management and debugging techniques for reliable Linux device-driver development. (K5)

Resources

1. Text Books

1. Simmonds, C. (2021). *Mastering Embedded Linux Programming* (3rd ed.). Packt Publishing.

2. Madieu, R. (2022). *Linux Device Driver Development: Develop Customized Drivers for Embedded Linux* (2nd ed.). Packt Publishing.

3. Vasudevan, J. (2021). *Linux Kernel Programming: A Comprehensive Guide to Kernel Internals, Writing Kernel Modules, and Kernel Synchronization.* Packt Publishing.

4. Ercoli, A. (2023). *Embedded Linux Systems with the Yocto Project.* Pearson Education.

5. Yaghmour, K., Masters, J., Ben-Yossef, G., & Gerum, P. (2021). *Building Embedded Linux Systems* (Updated ed.). O'Reilly Media.

2. Reference Books

1. Corbet, J., Rubini, A., & Kroah-Hartman, G. (2020). *Linux Device Drivers* (Updated ed.). O'Reilly Media.
2. Love, R. (2019). *Linux Kernel Development* (Updated ed.). Pearson Education.
3. Venkateswaran, S. (2019). *Essential Linux Device Drivers* (Updated ed.). Prentice Hall.
4. Bovet, D. P., & Cesati, M. (2020). *Understanding the Linux Kernel* (Updated ed.). O'Reilly Media.
5. Abbott, D. (2021). *Linux for Embedded and Real-time Applications* (4th ed.). Newnes.

3. E-Resources

1. NPTEL. (2023). *Embedded System Design and Architecture.* `https://nptel.ac.in/courses/106105159`
2. NPTEL. (2022). *System Software and Operating Systems.* `https://nptel.ac.in/courses/106105214`
3. Linux Kernel Organization. (2023). *Linux Kernel Driver Implementer's API Guide.* `https://www.kernel.org/doc/html/latest/driver-api/index.html`
4. Yocto Project. (2023). *Yocto Project Mega-Manual.* `https://docs.yoctoproject.org/singleindex.html`
5. Bootlin. (2023). *Embedded Linux and Kernel Engineering Training Materials.* `https://bootlin.com/docs/`

Industrial Relevance

The methodologies taught in this course bridge academic theory with current global semiconductor and hardware industrial deployment practices by equipping students with the exact skills required to develop Board Support Packages (BSPs) and kernel-level device drivers. As the industry rapidly transitions toward edge computing, advanced telecommunications, and automotive electronics, the ability to seamlessly integrate custom System-on-Chip (SoC) hardware with robust operating systems is paramount. Mastery of these vendor-neutral device tree configurations, driver synchronization techniques, and power management frameworks ensures graduates are prepared to tackle complex hardware-software co-design challenges directly relevant to commercial embedded system deployment and modern integrated circuit scaling.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	-	3	-	-	-	-	-	2	3	2	2
CO2	3	2	3	2	3	-	-	-	1	-	2	3	3	2
CO3	3	3	3	2	3	-	-	1	1	-	2	3	3	3
CO4	3	3	3	3	3	1	-	1	1	-	2	3	3	3
CO5	3	3	3	3	3	1	-	1	1	1	2	3	3	3
Weighted Average	3.00	2.60	2.80	2.50	3.00	1.00	-	1.00	1.00	1.00	2.00	3.00	2.80	2.60

Course Code: U23EVV71
Course Title: EMBEDDED COMMUNICATION PROTOCOLS
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design, Embedded Systems Architecture and Design
SDG: 9

Course Overview

This course provides a comprehensive understanding of wired, wireless, automotive, industrial, and IoT communication protocols utilized in modern embedded systems and System-on-Chip (SoC) architectures. It thoroughly examines protocol architectures, frame formats, timing, arbitration, error handling, and performance metrics across various short-range and long-range communication standards. Furthermore, the curriculum emphasizes hardware-software co-design, interface IP integration, and secure protocol bridging essential for developing robust edge-computing devices and IoT gateways.

Course Objectives

1. Analyze the architectural principles, timing characteristics, and operational mechanisms of synchronous and asynchronous serial communication interfaces for embedded applications.
2. Evaluate automotive, industrial, USB, and Ethernet network architectures to design deterministic, fault-tolerant communication systems.
3. Compare and integrate wireless technologies and IoT messaging protocols to architect secure, energy-efficient connected platforms and gateways.

Unit I: SERIAL COMMUNICATION INTERFACES **9 Hours**
Embedded communication architectures – Communication interface requirements in embedded systems and SoCs – Synchronous and asynchronous communication – Serial communication principles – UART architecture and frame format – RS-232, RS-422 and RS-485 – SPI architecture, modes and timing – I^2C architecture, addressing and bus operation – Bus arbitration and error handling – Data-rate and timing considerations – Communication interface IP and hardware implementation considerations – Selection of serial communication interfaces for embedded applications.
Active Learning Activity: Simulation-based analysis of UART, SPI and I^2C timing diagrams, addressing and bus arbitration using an open-source protocol-analysis environment.

Unit II: AUTOMOTIVE AND INDUSTRIAL COMMUNICATION **9 Hours**
Automotive communication requirements – Controller Area Network (CAN) architecture – CAN message and frame formats – CAN bus arbitration – Identifier-based priority – Error detection and error handling – Fault confinement – CAN FD – Local Interconnect Network (LIN) – Automotive Ethernet concepts – Industrial communication requirements – Modbus RTU – Modbus TCP – Industrial Ethernet concepts – Deterministic and real-time communication – Communication reliability and fault tolerance – Selection of automotive and industrial communication protocols.
Active Learning Activity: Construction and analysis of CAN and Modbus communication frames with arbitration and error-detection modeling using an open-source network simulation environment.

Unit III: USB AND ETHERNET COMMUNICATION **9 Hours**

USB architecture – USB topology – Host, device and hub – Endpoints and pipes – USB transfer types – USB enumeration process – Device classes – Embedded USB applications – Ethernet architecture – MAC and PHY concepts – Ethernet frame format – Ethernet addressing – TCP/IP protocol suite – IP addressing – TCP and UDP – Socket communication concepts – Embedded Ethernet applications – Protocol analysis and debugging – Hardware/software interface considerations for embedded communication.

Active Learning Activity: Protocol-analysis exercise involving USB enumeration and endpoint transactions and inspection of Ethernet frames and TCP/UDP communication using an open-source packet-analysis tool.

Unit IV: WIRELESS EMBEDDED COMMUNICATION **9 Hours**

Wireless communication requirements for embedded systems – Wireless communication architectures – IEEE 802.15.4 – Zigbee architecture and network topology – Bluetooth Low Energy (BLE) architecture – BLE advertising and connection procedures – BLE services and characteristics – Wi-Fi fundamentals – Wireless network architectures – Comparison of range, data rate, latency, reliability and power consumption – Wireless communication selection criteria – Embedded wireless applications – Energy-efficient wireless communication – Integration of wireless interfaces with embedded SoC platforms.

Active Learning Activity: Comparative performance analysis of BLE, Zigbee and Wi-Fi based on latency, throughput, range and energy consumption using an open-source wireless-network emulation environment.

Unit V: IoT COMMUNICATION AND PROTOCOL INTEGRATION **9 Hours**

IoT communication architecture – Machine-to-Machine (M2M) communication – Device-to-device and device-to-cloud communication – MQTT architecture – Publisher-subscriber model – MQTT broker and topics – Quality of Service (QoS) levels – CoAP architecture – RESTful communication – Protocol selection for constrained devices – Embedded IoT gateways – Protocol conversion and bridging – Communication security fundamentals – Authentication and secure communication concepts – Protocol analysis and debugging – Communication protocol integration in SoC and embedded systems – Case studies in automotive, industrial and IoT applications.

Active Learning Activity: Case-study-based design and analysis of an embedded IoT gateway involving MQTT-to-CoAP or MQTT-to-REST protocol conversion using an open-source IoT emulation environment.

Course Outcomes (COs)

Upon completion of the course, the students will be able to:

CO1: Apply architectural principles, timing parameters and interface characteristics to determine suitable synchronous and asynchronous serial communication interfaces for embedded and SoC applications. (K3)

CO2: Analyze frame structures, arbitration mechanisms, error detection and fault-confinement techniques of automotive and industrial communication protocols. (K4)

CO3: Analyze USB and Ethernet architectures, protocol layers, transfer mechanisms and communication processes for embedded applications. (K4)

CO4: Analyze and compare wireless communication technologies based on topology, range, data rate, latency, reliability and power consumption for embedded applications. (K4)

CO5: Evaluate IoT communication protocols and protocol-integration approaches for secure and efficient embedded gateway and SoC applications. (K5)

Resources

1. Text Books

1. Vahid, F., & Givargis, T. (2020). *Embedded System Design: A Unified Hardware/Software Introduction* (3rd ed.). Wiley.
2. Kamal, R. (2020). *Embedded Systems: Architecture, Programming and Design* (4th ed.). McGraw-Hill Education.
3. Hersent, O., Boswarthick, D., & Elloumi, O. (2022). *The Internet of Things: Key Applications and Protocols* (2nd ed.). Wiley.
4. Valvano, J. W. (2021). *Embedded Systems: Real-Time Interfacing to ARM Cortex-M Microcontrollers* (6th ed.).
5. Axelson, J. (2022). *USB Complete: The Developer's Guide* (5th ed.). Lakeview Research.

2. Reference Books

1. Di Natale, M., Zeng, H., Giusto, P., & Ghosal, A. (2020). *Understanding and Using Controller Area Network Communication Protocol: Theory and Practice*. Springer.
2. Kozierok, C. M. (2019). *The TCP/IP Guide: A Comprehensive, Illustrated Internet Protocols Reference*. No Starch Press.
3. Lea, P. (2020). *Internet of Things for Architects*. Packt.
4. Marwedel, P. (2021). *Embedded System Design: Embedded Systems Foundations of Cyber-Physical Systems*. Springer.
5. Noergaard, T. (2019). *Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers*. Newnes.

3. E-Resources

1. NPTEL. (2022). Embedded System Design with ARM. Note: Architectural interfaces and programming.
   `https://nptel.ac.in/courses/106105193`
2. NPTEL. (2023). Industrial Internet of Things. Note: MQTT, CoAP and Industrial Protocols.
   `https://nptel.ac.in/courses/106105195`
3. CAN in Automation (CiA). (2023). CAN technical resources. Note: CAN FD specifications.
   `https://www.can-cia.org`
4. USB Implementers Forum (USB-IF). (2023). USB developer resources. Note: USB architecture and classes.
   `https://www.usb.org`
5. IEEE Standards Association. (2023). IEEE 802.15.4 and wireless communication standards. Note: Zigbee and BLE architectures.
   `https://standards.ieee.org`

Industrial Relevance

Embedded communication protocols form a fundamental part of modern SoCs, electronic control units, automotive systems, industrial automation platforms, IoT gateways, and edge-computing devices. CAN FD, Automotive Ethernet, Modbus TCP, USB, Ethernet, BLE, Zigbee, Wi-Fi, MQTT, and CoAP are widely deployed for connecting sensors, controllers, processors, and intelligent edge nodes in modern semiconductor industries. This course develops critical skills relevant to the global electronics industry, including communication-interface IP development, protocol verification, embedded firmware design, and hardware/software co-design. The emphasis on timing, arbitration, fault handling, protocol analysis, and interface selection equips engineering graduates to architect and evaluate highly reliable communication infrastructures for next-generation automotive, industrial, and IoT applications.

CO-PO-PSO Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	-	2	-	-	-	-	-	-	3	2	-
CO2	3	3	2	2	2	-	-	-	-	-	-	3	2	-
CO3	3	3	2	2	2	-	-	-	-	-	-	3	2	-
CO4	3	3	2	2	-	-	-	-	-	-	-	3	2	2
CO5	3	3	3	3	3	2	-	-	-	-	2	3	2	3
Weighted Average	3.00	2.80	2.20	2.25	2.25	2.00	-	-	-	-	2.00	3.00	2.00	2.50

Course Code: U23EVV72
Course Title: INTERNET OF THINGS SYSTEM DESIGN
Course Type: Professional Elective
L–T–P–C: 3–0–0–3
Total Hours: 45
Prerequisites: Digital System Design, Computer Architecture and On-Chip Communication
SDG: 9

Course Overview

This course establishes the fundamental principles and architectural frameworks required for developing Internet of Things (IoT) systems. It comprehensively covers the technical themes of sensor integration, edge processing, communication protocols, security mechanisms, and hardware-software co-design. The knowledge gained enables engineers to develop scalable and secure IoT solutions relevant to the modern semiconductor, industrial automation, and connected electronics industries.

Course Objectives

1. Apply sensor interfacing, data acquisition, and low-power techniques to edge-device configurations.
2. Analyze IoT architectures, connectivity protocols, and security frameworks to select suitable technologies for specific applications.
3. Evaluate end-to-end IoT system designs by integrating hardware, software, and communication components while balancing performance trade-offs.

Unit I: IoT Architecture and Design Principles **9 Hours**
IoT characteristics and requirements – physical and logical design – functional blocks – things and smart objects – sensors and actuators – edge devices and gateways – reference architectures and models – deployment models – device identification and addressing – design constraints.
Active Learning Activity: Conceptual Simulation mapping physical and logical design components for a smart home application infrastructure.

Unit II: IoT Devices, Sensing and Edge Processing **9 Hours**
IoT device architecture – embedded platforms – sensor and actuator interfacing – analog and digital interfaces – data acquisition – signal conditioning – sampling and conversion – edge processing – filtering and aggregation – low-power operation.
Active Learning Activity: Technology Comparison of various embedded platform architectures based on power consumption and edge processing capabilities.

Unit III: IoT Connectivity and Data Exchange **9 Hours**
Short-range communication for IoT – Bluetooth Low Energy (BLE) – Zigbee – Wi-Fi – connectivity selection based on range, data rate and power – device-to-device and device-to-gateway communication – MQTT – CoAP – RESTful data exchange – edge-to-cloud communication.
Active Learning Activity: Data Analysis of packet overhead, bandwidth utilization, and latency variations between MQTT and CoAP protocols under constrained network conditions.

Unit IV: IoT Security and Device Management **9 Hours**
IoT security requirements – threats and vulnerabilities – authentication and authorization –

confidentiality and integrity – secure communication – security for resource-constrained devices – device identity and provisioning – secure boot – firmware integrity – secure updates and over-the-air (OTA) protocols – device lifecycle management.
Active Learning Activity: Failure Analysis evaluating the system-level impact of unauthorized access in a resource-constrained edge device and proposing mitigation strategies.

Unit V: End-to-End IoT System Design **9 Hours**
IoT system requirements – sensor and hardware selection – embedded processing and communication selection – gateway and edge-cloud integration – hardware-software co-design – system integration – energy, latency, reliability and scalability trade-offs – system testing and validation – selected IoT case studies.
Active Learning Activity: Design Review of an end-to-end IoT architecture for an industrial automation system, systematically highlighting integration challenges and system-level trade-offs.

Course Outcomes

CO1: Apply fundamental IoT architectures, reference models, and system-level design constraints to connected object configurations. (K3)

CO2: Analyze sensor interfacing, signal conditioning, and edge processing techniques for low-power IoT device architectures. (K4)

CO3: Analyze short-range communication technologies and application-layer protocols to select optimal connectivity solutions. (K4)

CO4: Analyze security threats, authentication frameworks, and lifecycle management protocols for resource-constrained IoT devices. (K4)

CO5: Evaluate end-to-end IoT system designs by assessing hardware-software co-design, integration strategies, and performance trade-offs. (K5)

Resources

1. Text Books

1. Bahga, A., & Madisetti, V. (2014). *Internet of Things: A Hands-On Approach*. VPT.
2. Serpanos, D., & Wolf, M. (2017). *Internet-of-Things (IoT) Systems: Architectures, Algorithms, Methodologies*. Springer.
3. Perry, L. (2015). *Internet of Things for Architects: Architecting IoT solutions by implementing sensors, communication infrastructure, edge computing, analytics, and security*. Packt Publishing.
4. Sinclair, B. (2017). *IoT Inc: How Your Company Can Use the Internet of Things to Win in the Outcome Economy*. McGraw-Hill Education.
5. Greengard, S. (2015). *The Internet of Things*. MIT Press.

2. Reference Books

1. Hersent, O., Boswarthick, D., & Elloumi, O. (2012). *The Internet of Things: Key Applications and Protocols*. John Wiley & Sons.

2. Buyya, R., & Dastjerdi, A. V. (Eds.). (2016). *Internet of Things: Principles and Paradigms*. Morgan Kaufmann.

3. Hanes, D., Salgueiro, G., Grossetete, P., Barton, R., & Henry, J. (2017). *IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things*. Cisco Press.

4. Lea, P. (2018). *Internet of Things for Architects*. Packt Publishing.

5. Russell, B., & Van Duren, D. (2016). *Practical Internet of Things Security*. Packt Publishing.

3. E-Resources

1. NPTEL – Introduction to Internet of Things: Comprehensive lectures on IoT concepts. `https://nptel.ac.in/courses/106105166`

2. MIT OpenCourseWare – IoT Systems: Advanced architectural concepts. `https://ocw.mit.edu/courses/iot`

3. IEEE Internet of Things – Technical Community and Research: Latest standards and whitepapers. `https://iot.ieee.org`

4. NIST – Internet of Things (IoT) Cybersecurity: Guidelines for secure IoT deployment. `https://www.nist.gov/programs-projects/internet-things-iot`

5. Coursera – Internet of Things (IoT) Specialization: Industry-oriented foundational courses. `https://www.coursera.org/specializations/iot`

Industrial Relevance

The curriculum aligns with contemporary demands in the semiconductor and connected electronics sectors by providing comprehensive training in IoT system architectures, low-power edge computing, and secure data exchange. Modern VLSI design increasingly focuses on hardware-software co-design for edge devices, requiring engineers to integrate sensor arrays, embedded processors, and secure communication protocols efficiently. By addressing energy, latency, and scalability trade-offs within a rigorous engineering framework, this course equips graduates to develop robust, resource-constrained IoT solutions that meet stringent industry standards for industrial automation, automotive electronics, and smart infrastructure deployments.

CO-PO-PSO Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	–	–	–	–	–	–	–	–	2	–	1
CO2	3	3	2	–	2	–	–	–	–	–	–	3	1	2
CO3	3	3	2	2	2	–	–	–	–	–	–	2	1	2
CO4	3	3	2	–	–	2	2	–	–	–	–	2	2	2
CO5	3	3	3	2	2	–	–	–	–	2	2	3	3	3
Weighted Average	**3.00**	**2.80**	**2.00**	**2.00**	**2.00**	**2.00**	**2.00**	**–**	**–**	**2.00**	**2.00**	**2.40**	**1.75**	**2.00**

Course Code: U23EVV73
Course Title: EDGE COMPUTING SYSTEMS
Course Type: Professional Elective
Prerequisites: Digital System Design, Embedded Systems
L T P C: 3 0 0 3
SDG: SDG 9: Industry, Innovation, and Infrastructure

Course Overview

This course explores the architectural foundations, virtualization paradigms, and resource management strategies underpinning modern edge and fog computing systems. Students will investigate computation offloading, distributed data management, and secure hardware-software integration for latency-sensitive applications. The curriculum bridges theoretical distributed systems with practical silicon-level implementations, preparing engineers to design intelligent, energy-efficient edge-cloud infrastructures.

Course Objectives

1. Explain the fundamentals, architectures, and operational characteristics of edge, fog, and cloud computing environments.
2. Analyze computation offloading, task partitioning, and resource-management strategies under strict latency and energy constraints.
3. Design optimized edge-cloud architectures integrating hardware-aware virtualization and real-time edge artificial intelligence systems.

Unit I: Edge Computing Fundamentals and Architectures **9 Hours**
Introduction to Edge Computing – Cloud Computing Fundamentals – Edge–Cloud Continuum – Fog Computing – Edge Reference Architectures – Edge Nodes and Gateways – Edge Data Centers – Latency and Bandwidth Requirements – Applications and Challenges.
Active Learning Activity: Flipped Classroom session analyzing real-world latency profiles across multi-tier fog and cloud infrastructures using open-source network simulation frameworks.

Unit II: Edge Platforms and Virtualization **9 Hours**
Edge Computing Platforms – Resource-Constrained Edge Devices – Virtualization Fundamentals – Hardware-Assisted Virtualization – Lightweight Virtualization – Container-Based Edge Computing – Container Orchestration – Hardware-Aware Virtualization – Edge Service Deployment.
Active Learning Activity: Simulation-based lab deploying lightweight container models on resource-constrained simulated edge nodes to evaluate memory and energy overheads.

Unit III: Computation Offloading and Resource Management **9 Hours**
Computation Offloading Fundamentals – Full and Partial Offloading – Task Partitioning Strategies – Offloading Decision Making – Edge Task Scheduling – Resource Allocation – Energy-Aware Edge Computing – Latency-Aware Resource Management – Distributed Edge Resource Management.
Active Learning Activity: Collaborative group problem-solving designing heuristic scheduling algorithms for partitioned task graphs under strict latency bounds.

Unit IV: Edge Data Management and Security **9 Hours**
Edge Data Management Fundamentals – Data Placement and Locality – Edge Data Processing – Data Caching at the Edge – Distributed Data Management – Edge Data Privacy – Security Threats in Edge Computing – Authentication and Access Control – Secure Communication.

Active Learning Activity: Case study analysis evaluating distributed data placement strategies and cryptographic access control protocols for compromised edge nodes.

Unit V: Edge-Cloud System Design and Edge AI **9 Hours**

Edge–Cloud System Design – Hardware–Software Co-Design – Edge AI Fundamentals – AI Accelerator Integration – Hardware-Aware Edge AI – Real-Time Edge Applications – Edge SoC Architectures – Performance and Energy Optimization – Emerging Edge Systems.

Active Learning Activity: Design project modeling a hardware-accelerated edge inference node using open-source architecture simulation tools to optimize throughput and energy efficiency.

Course Outcomes (COs)

CO1: Explain edge, fog and cloud computing architectures, reference models and operational characteristics for distributed computing environments. (K2)

CO2: Apply virtualization, containerization and service-deployment techniques to resource-constrained edge platforms. (K3)

CO3: Analyze computation-offloading, task-partitioning, scheduling and resource-management strategies considering latency, bandwidth and energy constraints. (K4)

CO4: Evaluate distributed data-management and security mechanisms for reliable and secure edge-computing environments. (K5)

CO5: Design optimized edge-cloud architectures for real-time IoT and intelligent edge applications considering latency, energy, reliability and hardware-software integration constraints. (K6)

Resources

1. Text Books

1. Buyya, R., & Satyanarayanan, S. (2019). *Edge computing: Fundamentals, advances and applications*. Morgan Kaufmann.
2. Mao, Y., You, C., Zhang, J., Huang, K., & Letaief, K. B. (2020). *A survey on mobile edge computing: The communication perspective*. Cambridge University Press.
3. Shi, W., Dustdar, S., & Wu, J. (2021). *Edge computing: A primer*. Springer.
4. Zhang, Y., Chen, M., Sahinoglu, Z., & Wang, W. (2022). *Handbook of smart cities: Software, services, and systems*. Springer.
5. Mahmood, Z. (2023). *Cloud-edge and fog-based computing: Paradigms, methodologies, and applications*. Auerbach Publications.

2. Reference Books

1. Mukherjee, M., Lloret, J., & Shojafar, M. (2019). *Principles of fog computing: Toward the networked edge*. Wiley-IEEE Press.
2. Salah, K., Rehman, M. H., Nizamuddin, N., & Al-Fuqaha, A. (2020). *Blockchain for edge computing: Paradigms and security*. CRC Press.
3. Pati, S. (2021). *Fog and edge computing: Principles and paradigms*. Wiley.
4. Hwang, K., & Fox, G. C. (2022). *Distributed and cloud computing: From parallel processing to the internet of things*. Morgan Kaufmann.

5. Aggarwal, C. C. (2023). *Artificial intelligence at the edge: Algorithms, architectures, and applications*. Springer.

3. E-Resources

1. National Programme on Technology Enhanced Learning (NPTEL). *Course on Cloud and Edge Computing*. Note: Focus on architecture, containerization, and offloading models.
   `https://nptel.ac.in/courses/106105167`
2. IEEE Computer Society. *Edge Computing Community Resources and Webinars*. Note: Covers emerging hardware accelerators and edge intelligence frameworks.
   `https://www.computer.org/publications/tech-shorts/edge-computing`
3. Cloud Native Computing Foundation (CNCF). *Documentation on Lightweight Container Orchestration*. Note: Reference for resource-constrained environment deployments.
   `https://www.cncf.io/projects/`
4. Open Source Infrastructure Simulation Project. *System-Level Architecture Simulation Framework Documentation*. Note: Used for modeling hardware-software co-design and offloading.
   `https://www.gem5.org/documentation/`
5. Network Simulation Community. *Simulation of Heterogeneous Edge Networks*. Note: Documentation on latency and bandwidth metrics.
   `https://www.nsnam.org/docs/`

Industrial Relevance

The rapid proliferation of Internet of Things deployments, autonomous systems, and real-time artificial intelligence requires computational processing to move closer to data sources, shifting workloads from centralized datacenters to distributed edge infrastructures. This course directly bridges academic distributed computing theory with global semiconductor and hardware deployment practices by addressing hardware-software co-design, resource-constrained virtualization, and energy-aware edge system optimization. Industry engineers equipped with these competencies can architect high-performance, low-latency silicon systems and edge SoCs that satisfy the stringent efficiency, reliability, and security demands of next-generation intelligent electronic systems.

CO-PO-PSO Articulation Matrix

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	-	1	-	-	-	-	-	1	2	1	2
CO2	3	3	2	1	2	-	-	-	-	-	1	3	2	2
CO3	3	3	3	2	2	1	-	-	-	-	2	3	2	3
CO4	2	3	2	2	1	1	1	-	-	-	1	2	2	2
CO5	3	3	3	3	3	1	1	1	1	1	2	3	3	3
Weighted Average	2.80	2.80	2.20	2.00	1.80	1.00	1.00	1.00	1.00	1.00	1.40	2.60	2.00	2.40

Course Code: U23EVV74
Course Title: EMBEDDED AI AND TINYML
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design, Embedded Systems Architecture and Design
SDG: 9

Course Overview

This course introduces the principles and methodologies for deploying artificial intelligence and machine learning algorithms on ultra-low-power, resource-constrained embedded and edge platforms. It covers embedded AI fundamentals, lightweight neural-network architectures, model optimization techniques, and on-device deployment workflows. Emphasis is placed on the co-optimization of machine-learning models and embedded hardware considering memory, latency, energy, and accuracy constraints for diverse engineering applications.

Course Objectives

1. To analyze the computational, memory, latency, and energy constraints of lightweight neural-network architectures on resource-constrained embedded inference platforms.
2. To apply model quantization, pruning, knowledge distillation, and compression techniques for optimizing edge intelligence models.
3. To design and deploy end-to-end embedded artificial intelligence sensor-to-inference pipelines for real-time industrial and healthcare applications.

Unit I: EMBEDDED ARTIFICIAL INTELLIGENCE FUNDAMENTALS 9 Hours
Introduction to Embedded AI - Edge AI and TinyML - Motivation for on-device intelligence - Embedded machine-learning workflow - Supervised and unsupervised learning concepts - Classification and regression - Feature extraction and feature selection - Training, validation and inference - Embedded inference - Computational requirements - Memory requirements - Latency, energy and accuracy constraints - Resource-constrained AI systems - Embedded AI hardware platforms - Microcontroller and edge-processor considerations - AI inference constraints in SoC-based embedded systems.
Active Learning Activity: Analyze the memory footprint, computational requirements and energy consumption of representative classification models on resource-constrained edge processor architectures using an open-source instruction-level simulation environment.

Unit II: NEURAL NETWORKS FOR EMBEDDED SYSTEMS 9 Hours
Artificial neural networks - Perceptron - Multilayer neural networks - Activation functions - Feed-forward inference - Computational requirements of neural-network inference - Convolutional Neural Networks - Convolution operation - Pooling - Feature maps - CNN-based classification - Time-series and sensor-data processing - Lightweight neural-network architectures - MobileNet concepts - Depthwise separable convolution - Computational complexity reduction - Neural-network inference on resource-constrained systems - Accuracy, latency and memory metrics.
Active Learning Activity: Mathematically model and compare standard and depthwise separable convolution operations and quantify their computational and parameter reductions for embedded inference.

Unit III: TINYML AND MODEL OPTIMIZATION **9 Hours**

TinyML concepts and workflow - Constraints of microcontroller-based machine learning - Model size and memory footprint - Computational complexity - Model quantization - Post-training quantization - Integer quantization - Quantization-aware training concepts - Weight pruning - Model sparsity - Model compression - Knowledge distillation concepts - Memory optimization - Operator optimization - Accuracy, latency, memory and energy trade-offs - Model profiling - Benchmarking and optimization for embedded inference.

Active Learning Activity: Perform model quantization and weight-pruning experiments using an open-source model-optimization framework and evaluate accuracy, memory footprint, inference latency and energy-related trade-offs.

Unit IV: TINYML DEPLOYMENT ON EMBEDDED PLATFORMS **9 Hours**

TinyML development workflow - Dataset and model preparation - Model conversion - Embedded model representation - Microcontroller inference framework concepts - Embedded inference runtime - Tensor arena - Memory allocation - Optimized inference kernels - Microcontroller neural network library concepts - Sensor data acquisition - Data preprocessing - Feature generation - On-device inference - Inference latency profiling - Memory profiling - Power-aware inference - Runtime optimization - Debugging and validation of TinyML applications.

Active Learning Activity: Deploy a lightweight neural-network model on an emulated microcontroller platform and analyze tensor-arena utilization, inference latency and memory requirements using an embedded inference runtime.

Unit V: EMBEDDED AI SYSTEM DESIGN AND APPLICATIONS **9 Hours**

End-to-end Embedded AI system design - Sensor-to-inference pipeline - System requirements - Hardware and model selection - Embedded processor and memory selection - Real-time AI inference - Event-driven intelligent systems - Always-on sensing - Keyword spotting - Anomaly detection - Human activity recognition - Predictive maintenance - Intelligent condition monitoring - Embedded vision concepts - Smart healthcare and wearable applications - Industrial Embedded AI - Automotive Embedded AI - Privacy-preserving on-device intelligence - Hardware/software co-design considerations - Energy, latency, memory and accuracy trade-offs - Embedded AI system design case studies.

Active Learning Activity: Design and evaluate a low-power, event-driven Embedded AI system for industrial anomaly detection or predictive maintenance, including sensor acquisition, preprocessing, inference and performance evaluation.

Course Outcomes

Upon completion of the course, the students will be able to:

CO1: Analyze Embedded AI principles and evaluate computational, memory, latency, and energy constraints of resource-constrained edge hardware. (K4)

CO2: Analyze lightweight neural-network architectures for efficient processing of sensor and time-series data on embedded platforms. (K4)

CO3: Apply quantization, pruning, knowledge distillation, and model-compression techniques to optimize machine learning models for embedded inference. (K3)

CO4: Apply deployment workflows to convert, deploy, and profile optimized inference models on microcontroller-based hardware frameworks. (K3)

CO5: Design end-to-end Embedded AI sensor-to-inference pipelines for real-time industrial, automotive, and healthcare applications considering hardware constraints. (K6)

Resources

1. Text Books

1. Warden, P., & Situnayake, D. (2019). *Tiny Machine Learning for Edge Devices*. O'Reilly Media.

2. Sharma, R. (2020). *Machine Learning for Embedded Systems: Advancing Edge Intelligence*. Apress.

3. Ray, S., & Dutta, A. (2023). *Embedded Machine Learning for Smart Edge Devices: Architecture and Implementation*. Springer.

4. Plunkett, J. (2021). *Edge AI and Embedded Intelligence: Build Smart IoT Devices with Machine Learning*. Packt.

5. Soro, S. (2022). *Tiny Machine Learning and Edge Computing: Algorithms and Architectures*. CRC Press.

2. Reference Books

1. Janapa Reddi, V., & John, L. K. (2021). *Machine Learning Systems: Design and Implementation for Edge Computing*. Morgan & Claypool.

2. Banbury, C. (2023). *Benchmarking Embedded AI Systems: Challenges and Methodologies for Low-Power Intelligence*. IEEE Press.

3. Suda, N. (2021). *Deep Learning on Microcontrollers: Optimization and Deployment Techniques*. Cambridge University Press.

4. Zhou, Z., Chen, X., Li, E., Zeng, L., & Luo, K. (2019). *Edge Intelligence: Paving the Last Mile of Artificial Intelligence with Edge Computing*. Wiley.

5. Rogers, P., & Lewis, M. (2022). *Ultra-Low-Power AI for Edge Platforms*. Elsevier.

3. E-Resources

1. NPTEL Course on Artificial Intelligence for Edge Devices. Note: Hardware Constraints and Optimization.
   `https://nptel.ac.in/courses/106105195`

2. Harvard University Educational Resources on Embedded Machine Learning. Note: Fundamentals and Deployment.
   `https://tinyml.seas.harvard.edu/`

3. Open-source Microcontroller Neural Network Library Documentation. Note: Kernel Optimization and Integration.
   `https://developer.arm.com/architectures/instruction-sets/dsp-extensions`

4. Embedded Inference Framework Developer Guide. Note: Model Conversion and Tensor Allocation.
   `https://www.tensorflow.org/lite/microcontrollers`

5. Edge AI Foundation Educational Resources and Benchmarks. Note: Industry Standards and Profiling.
   `https://www.mlcommons.org/en/training-tiny/`

Industrial Relevance

Embedded AI and TinyML enable machine-learning inference directly on resource-constrained microcontrollers, embedded processors, and edge architectures. This course addresses critical industry requirements for low-power intelligent systems by integrating neural-network optimization, memory-aware inference, model compression, and sensor-to-inference system design. The knowledge developed through this curriculum is highly relevant to semiconductor and embedded industries working on AI-enabled system-on-chips, edge accelerators, automotive electronics, industrial automation, and predictive maintenance. By emphasizing quantization, pruning, latency profiling, and energy-aware inference, students acquire the necessary engineering competencies to bridge the gap between machine-learning algorithms and physical hardware constraints in real-world deployment scenarios.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	1	-	-	-	-	-	-	2	2	1	2
CO2	3	3	2	2	-	-	-	-	-	-	2	3	1	2
CO3	3	2	3	2	3	-	-	-	-	-	2	3	2	2
CO4	3	2	3	2	3	-	-	-	-	-	2	3	3	2
CO5	3	3	3	3	3	2	1	2	2	2	3	3	3	3
Weighted Average	3.00	2.60	2.60	2.00	3.00	2.00	1.00	2.00	2.00	2.00	2.20	2.80	2.00	2.20

Course Code: U23EVV75
Course Title: DATA CONVERTER DESIGN
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Linear Integrated Circuits, CMOS VLSI Design
SDG: 4, 9

Course Overview

This course provides an in-depth understanding of the analysis, architecture, and CMOS implementation of data converters used in modern mixed-signal systems. It covers fundamental performance metrics, static and dynamic nonidealities, diverse DAC architectures, SAR and pipeline ADCs, alongside oversampling methodologies and comprehensive testing techniques. Emphasis is placed on resolving critical trade-offs related to resolution, speed, power, area, noise, and reliability relevant to advanced mixed-signal integrated circuits and System-on-Chip applications.

Course Objectives

1. To analyze data-converter performance metrics, nonidealities, and architectural trade-offs inherent in mixed-signal system design.
2. To design and optimize CMOS DAC, SAR ADC, and pipeline ADC architectures considering energy efficiency, resolution, and layout constraints.
3. To evaluate advanced oversampling techniques, calibration methodologies, and silicon-level testing strategies for integrated data converters under diverse variations.

Unit I: DATA CONVERTER PERFORMANCE AND NONIDEALITIES 9 Hours
Sampling process, quantization process and quantization characteristics - Quantization error, quantization noise and resolution - Static converter errors and their effects - Differential and integral nonlinearity and missing-code behavior - Dynamic performance parameters - Effective resolution and usable signal range - Timing uncertainty and its impact on conversion accuracy - Noise sources and mismatch-related errors - Speed, resolution, power, area and overall converter performance.
Active Learning Activity: Behavioral simulation of quantization noise and clock-jitter effects on SNR and converter performance using an open-source numerical analysis environment.

Unit II: CMOS DAC ARCHITECTURES AND DESIGN 9 Hours
DAC operation, specifications and architecture selection - Capacitive and charge-scaling DAC principles - Current-cell architecture and high-speed operation - Coding methods and implementation trade-offs - Segmentation strategies and performance benefits - Current-source accuracy and finite output resistance - Switching transients, glitches and settling behavior - DEM techniques and mismatch mitigation - Common-centroid layout, routing, matching and design trade-offs.
Active Learning Activity: Analyze DAC current-cell mismatch and develop a conceptual common-centroid layout strategy using an open-source circuit and layout environment.

Unit III: SAR AND PIPELINE ADC DESIGN 9 Hours
Successive approximation principle and conversion sequence - CDAC architecture and implementation - Charge redistribution and energy-efficient switching - Comparator operation, speed

and resolution requirements - Comparator nonidealities and their effects - Reference accuracy and CDAC mismatch - Low-energy switching strategies - Sub-ADC, sub-DAC, residue amplifier and inter-stage operation - Gain error, mismatch and digital correction techniques.
Active Learning Activity: Design and simulate an energy-efficient charge-redistribution switching sequence for a SAR ADC and evaluate its conversion behavior using general-purpose simulation tools.

Unit IV: OVERSAMPLING AND NOISE-SHAPING CONVERTERS 9 Hours
Oversampling concept and resolution improvement - Noise-shaping principle and spectral distribution - Basic modulation principles - Architecture and operation of first-order modulators - Multi-order loop structures and performance - STF and NTF analysis - Stability considerations and quantizer architectures - Architectural comparison and implementation considerations - Digital filtering and Sigma-Delta ADC and DAC applications.
Active Learning Activity: Simulate the STF, NTF and stability characteristics of a Sigma-Delta modulator using an open-source signal-processing environment.

Unit V: DATA CONVERTER CALIBRATION AND TESTING 9 Hours
Sources of converter errors and need for calibration - Correction of offset and gain errors - DNL and INL correction and component-mismatch compensation - Calibration architectures and operating principles - Digital-assisted calibration techniques - Static converter characterization and histogram-based testing - Extraction of static linearity parameters - Coherent sampling, FFT analysis and dynamic testing - Dynamic performance measurement and PVT evaluation.
Active Learning Activity: Extract DNL, INL and ENOB from simulated converter output-code histograms and evaluate converter performance using open-source data-analysis tools.

Course Outcomes

CO1: Analyze data-converter performance metrics, nonidealities and architectural trade-offs under noise and mismatch conditions. (K4)
CO2: Design CMOS DAC architectures considering resolution, speed, power, mismatch and layout constraints. (K6)
CO3: Design SAR and pipeline ADC architectures considering energy-efficient switching, comparator limitations and digital error correction. (K6)
CO4: Analyze oversampling and noise-shaping converter architectures based on stability, noise-transfer characteristics and performance requirements. (K4)
CO5: Evaluate calibration and testing techniques for integrated data converters under process, voltage and temperature variations. (K5)

Resources

1. Text Books

1. Carusone, T. C., Johns, D. A., & Martin, K. W. (2022). *Analog Integrated Circuit Design* (3rd ed.). John Wiley & Sons.
2. Razavi, B. (2020). *Principles of Data Conversion System Design* (2nd ed.). IEEE Press.
3. Baker, R. J. (2019). *CMOS: Circuit Design, Layout, and Simulation* (4th ed.). John Wiley & Sons.
4. Maloberti, F. (2021). *Data Converters* (2nd ed.). Springer.
5. Pelgrom, M. J. (2022). *Analog-to-Digital Conversion* (3rd ed.). Springer.

2. Reference Books

1. Schreier, R., Pavan, S., & Temes, G. C. (2023). *Understanding Delta-Sigma Data Converters* (2nd ed.). IEEE Press.
2. Harpe, P., Cantatore, E., & van Roermund, A. (2020). *Ultra-Low-Power Analog Interfaces for IoT Applications*. Springer.
3. Allen, P. E., & Holberg, D. R. (2021). *CMOS Analog Circuit Design* (3rd ed.). Oxford University Press.
4. Jespers, P. G., & Murmann, B. (2021). *Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables*. Cambridge University Press.
5. Norsworthy, S. R., Schreier, R., & Temes, G. C. (2019). *Delta-Sigma Data Converters: Theory, Design, and Simulation*. IEEE Press.

3. E-Resources

1. NPTEL. (2022). *Analog Circuits and Systems through Integrated Circuit Design*. `https://nptel.ac.in/courses/108106105`
2. NPTEL. (2021). *VLSI Data Conversion Circuits*. `https://nptel.ac.in/courses/108106159`
3. NPTEL. (2023). *Mixed-Signal IC Design*. `https://nptel.ac.in/courses/108106099`
4. IEEE Solid-State Circuits Society. (2023). *Mixed-Signal Design Resources*. `https://sscs.ieee.org/resources`
5. Open Circuit Design. (2023). *Open-source mixed-signal simulation and layout resources*. `http://opencircuitdesign.com/`

Industrial Relevance

Data converters provide the critical interface between real-world analog signals and digital processing systems in modern mixed-signal ICs and System-on-Chip architectures. They are widely utilized in wireless communication, automotive electronics, radar, sensor interfaces, IoT systems, medical electronics, and edge-computing platforms. The course develops essential competencies in data-converter architecture selection, CMOS circuit design, mismatch-aware implementation, performance evaluation, calibration, and silicon-level testing, ensuring students are well-prepared to meet the demands of semiconductor industries involved in analog and mixed-signal IC design, IP development, and advanced hardware deployment.

CO-PO-PSO Articulation Matrix

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	1	2	-	-	-	-	-	1	3	2	1
CO2	3	3	3	2	3	1	-	1	1	1	2	3	3	2
CO3	3	3	3	2	3	1	-	1	1	1	2	3	3	2
CO4	3	3	2	2	2	-	-	-	-	-	1	3	2	2
CO5	3	3	2	3	3	1	1	1	2	1	2	3	3	2
Weighted Average	3.00	3.00	2.40	2.00	2.60	1.00	1.00	1.00	1.33	1.00	1.60	3.00	2.60	1.80

Course Code: U23EVV76
Course Title: PLL AND CLOCK GENERATION CIRCUITS
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Linear Integrated Circuits, Digital System Design
SDG: 9

Course Overview

This course provides a comprehensive understanding of phase-locked loops, voltage-controlled oscillators, frequency synthesizers, and clock-generation architectures used in modern VLSI and System-on-Chip systems. It covers critical theoretical and practical aspects, including PLL dynamics, phase detectors, charge-pump PLLs, frequency dividers, integer-N and fractional-N frequency synthesis, and delay-locked loops. Emphasis is strategically placed on evaluating stability, phase noise, jitter, frequency accuracy, power efficiency, and timing trade-offs in high-speed integrated environments.

Course Objectives

1. Analyze phase-locked loop dynamics, stability criteria, and fundamental performance parameters to design robust frequency synthesis systems.
2. Evaluate the architectures and nonidealities of phase detectors, charge pumps, voltage-controlled oscillators, and frequency dividers considering noise and power trade-offs.
3. Design advanced clock-generation and synchronization architectures for high-speed integrated SoC systems adhering to stringent jitter, skew, and timing requirements.

Unit I: PLL DYNAMICS AND PERFORMANCE **9 Hours**
PLL Fundamentals - Linear PLL Model - Phase and Frequency-Domain Analysis - Loop Dynamics and Bandwidth - Damping Factor and Stability - Lock Range and Capture Range - Phase Error and Acquisition - Phase Noise and Jitter - Reference Spurs and Performance Trade-offs.
Active Learning Activity: Derive a second-order PLL transfer function and simulate its step response, acquisition time and locking behavior using an open-source circuit-modeling environment.

Unit II: PHASE DETECTORS AND CHARGE-PUMP PLLs **9 Hours**
Phase Detector Fundamentals - XOR Phase Detector - Sequential Phase Detectors - Phase-Frequency Detector - Dead Zone and PFD Nonidealities - Charge Pump Architecture - Charge-Pump Nonidealities - Loop Filter Design - Charge-Pump PLL Design.
Active Learning Activity: Design and simulate a tri-state PFD and charge pump and analyze the effects of current mismatch and dead zone on PLL performance.

Unit III: VOLTAGE-CONTROLLED OSCILLATORS AND FREQUENCY DIVIDERS **9 Hours**
CMOS Oscillator Fundamentals - Ring Oscillators - LC Oscillators - Voltage-Controlled Oscillators - VCO Tuning Characteristics - VCO Phase Noise - Frequency Dividers - Prescalers and Programmable Dividers - Divider Design Trade-offs.
Active Learning Activity: Compare ring and LC VCO architectures through circuit simulation and evaluate tuning range, phase noise and power trade-offs.

Unit IV: FREQUENCY SYNTHESIZERS **9 Hours**

Frequency Synthesis Fundamentals - Integer-N Frequency Synthesizers - Frequency Resolution - Reference Frequency and Lock Time - Phase Noise and Reference Spurs - Fractional-N Frequency Synthesis - Accumulator-Based Fractional Division - Sigma-Delta Fractional-N Synthesis - Synthesizer Design Trade-offs.

Active Learning Activity: Model a fractional-N frequency synthesizer using an accumulator and first-order Sigma-Delta modulator and analyze quantization-noise shaping and spur characteristics.

Unit V: CLOCK GENERATION AND SYNCHRONIZATION **9 Hours**

Clock Generation Requirements - Clock Multiplication and Division - Delay-Locked Loops - Phase Interpolation - Clock and Data Recovery - Clock Jitter and Skew - Duty-Cycle Distortion and Buffers - Clock Distribution and Gating - SoC Clock Synchronization.

Active Learning Activity: Analyze an SoC clock-distribution network and DLL-based clocking system and evaluate clock skew, jitter and timing trade-offs.

Course Outcomes

CO1: Analyze PLL dynamics, stability, phase noise, jitter and performance characteristics. (K4)

CO2: Analyze phase detectors, charge pumps and loop filters for charge-pump PLL design. (K4)

CO3: Analyze VCO and frequency-divider architectures considering tuning range, phase noise, speed and power. (K4)

CO4: Analyze integer-N and fractional-N frequency synthesizer architectures considering resolution, phase noise, reference spurs and lock time. (K4)

CO5: Design clock-generation and synchronization architectures for integrated SoC systems considering jitter, skew, power and timing requirements. (K6)

Resources

1. Text Books

1. Razavi, B. (2020). *Design of Analog CMOS Integrated Circuits* (2nd ed.). McGraw-Hill Education.
2. Baker, R. J. (2019). *CMOS: Circuit Design, Layout, and Simulation* (4th ed.). Wiley.
3. Rogers, J., Plett, C., & Dai, F. (2022). *Integrated Circuit Design for High-Speed Frequency Synthesis* (2nd ed.). Artech House.
4. Gardner, F. M. (2021). *Phaselock Techniques* (3rd ed.). Wiley-Interscience.
5. Best, R. E. (2023). *Phase-Locked Loops: Design, Simulation, and Applications* (6th ed.). McGraw-Hill Professional.

2. Reference Books

1. Craninckx, J., & Steyaert, M. (2020). *Wireless CMOS Frequency Synthesizer Design.* Springer.
2. Banerjee, D. (2019). *PLL Performance, Simulation and Design* (5th ed.). National Semiconductor.

3. Egan, W. F. (2021). *Frequency Synthesis by Phase Lock* (3rd ed.). Wiley-IEEE.

4. Vani, P., & Kumar, E. V. (2022). *CMOS PLL Synthesizers: Analysis and Design.* CRC Press.

5. Karki, J. (2023). *Clock and Data Recovery for High-Speed Serial Links.* Artech House.

3. E-Resources

1. NPTEL. (2022). Phase-Locked Loops and Frequency Synthesizers. `https://nptel.ac.in/courses/117106115`

2. NPTEL. (2021). High-Speed Clock and Data Recovery Circuits. `https://nptel.ac.in/courses/117106087`

3. MIT OpenCourseWare. (2020). High-Speed Communication Circuits and Systems. `https://ocw.mit.edu/courses/electrical-engineering-and-computer-science`

4. IEEE Solid-State Circuits Society. (2023). Resources on PLL and DLL Design. `https://sscs.ieee.org/resources`

5. Open-Source EDA Documentation. (2022). Circuit Simulation and Modeling for PLLs. `https://ngspice.sourceforge.io/docs.html`

Industrial Relevance

PLL and clock-generation circuits form the fundamental timing backbone of modern System-on-Chip (SoC) architectures, microprocessors, and high-speed communication interfaces such as PCIe, USB, and DDR. This course directly bridges core analog design theory with industry-standard mixed-signal implementation practices, enabling engineers to systematically manage phase noise, mitigate timing jitter, and guarantee robust clock distribution across advanced semiconductor nodes. These highly specialized competencies seamlessly align with the immediate demands of the global semiconductor industry, where optimizing timing margins and power boundaries is paramount for developing next-generation edge-AI accelerators, advanced telecommunications infrastructure, and secure processing platforms.

CO-PO-PSO Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	2	-	-	-	-	-	1	3	2	2
CO2	3	3	2	2	2	-	-	-	-	-	1	3	2	2
CO3	3	3	2	2	3	-	-	-	-	-	1	3	3	2
CO4	3	3	3	2	2	-	-	-	-	-	2	3	3	2
CO5	3	3	3	3	3	1	-	2	2	1	2	3	3	3
Weighted Average	3.00	3.00	2.40	2.20	2.40	1.00	-	2.00	2.00	1.00	1.40	3.00	2.60	2.20

Course Code: U23EVV77
Course Title: POWER MANAGEMENT INTEGRATED CIRCUITS
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Linear Integrated Circuits, Electronic Devices and Circuits
SDG: 7, 9

Course Overview

This course provides a comprehensive understanding of the analysis, design, and optimization of Power Management Integrated Circuits (PMICs) used in energy-efficient VLSI and System-on-Chip systems. It deeply explores power-management fundamentals, covering linear regulators, switched-mode DC-DC converters, switched-capacitor architectures, and system-level control mechanisms. Furthermore, emphasis is placed on maximizing efficiency through careful management of power losses, feedback stability, transient response, thermal constraints, and Dynamic Voltage and Frequency Scaling (DVFS).

Course Objectives

1. Analyze power-management requirements, linear-regulator architectures, and feedback mechanisms to optimize efficiency and transient performance in integrated systems.
2. Evaluate the design, conduction modes, and control techniques of switched-mode DC-DC and switched-capacitor converters for effective power conversion.
3. Design comprehensive system-level PMIC architectures that seamlessly incorporate protection circuitry, power sequencing, power gating, and Dynamic Voltage and Frequency Scaling.

Unit I: FUNDAMENTALS OF POWER MANAGEMENT **9 Hours**

Power Management Requirements and Specifications – Supply-voltage requirements, current requirements, efficiency and reliability - Linear and Switching Regulators – Operating principles and architectural comparison - Power Efficiency and Loss Mechanisms – Conduction, switching and quiescent power losses - Power MOSFET Characteristics – On-resistance, threshold voltage, gate charge and switching behavior - Conduction and Switching Losses – Loss mechanisms and their dependence on load and switching frequency - Passive Components for PMICs – Inductor, capacitor and ESR considerations - Voltage and Current References – Reference generation and current-sensing principles - Line Regulation, Load Regulation and PSRR – Power-supply performance parameters - Thermal Management and PMIC Architectures – Thermal considerations and integrated power-management architectures.
Active Learning Activity: Simulate and compare conduction and switching losses of power MOSFETs under different load conditions using an open-source circuit simulator.

Unit II: LINEAR REGULATORS **9 Hours**

Linear Regulator Fundamentals – Architecture, operation and applications - Low-Dropout Regulator Architecture – LDO blocks and operating principles - Error Amplifier Design – Error amplification and feedback operation - Pass Transistor and Voltage Reference – Pass-device operation and reference requirements - Feedback Network and Regulation – Feedback mechanism, dropout voltage and regulation - Quiescent Current, Efficiency and PSRR – Performance metrics of integrated regulators - Frequency Response, Stability and Compensation – Loop

response, phase margin and compensation - Output Capacitor, ESR and Transient Response – Capacitor effects and line/load transients - Protection and Capacitorless LDOs – Current limiting, thermal protection and capacitorless LDO concepts.
Active Learning Activity: Design and simulate an LDO and characterize its stability, PSRR and line/load transient response using an analog circuit simulator.

Unit III: SWITCHED-MODE DC-DC CONVERTERS **9 Hours**
Switched-Mode Power Conversion Principles – Switching operation and energy transfer - Buck Converter – Architecture, operation and steady-state characteristics - Boost Converter – Architecture, operation and voltage conversion - Buck-Boost Converter – Operating modes and voltage conversion - Continuous and Discontinuous Conduction Modes – CCM/DCM operation and characteristics - Inductor and Capacitor Selection – Ripple current, ripple voltage and component requirements - Synchronous Rectification and Power Losses – Synchronous switching, conduction and switching losses - PWM and Feedback Control – Pulse-width modulation, voltage-mode and current-mode control - Compensation and Integrated DC-DC Converter Design – Feedback compensation, transient performance and IC implementation considerations.
Active Learning Activity: Model an open-loop and closed-loop synchronous buck converter and analyze inductor ripple, output-voltage regulation and transient response.

Unit IV: SWITCHED-CAPACITOR CONVERTERS **9 Hours**
Switched-Capacitor Power Conversion Principles – Charge transfer and capacitor-based energy conversion - Charge Pump Architecture – Basic charge-pump operation and applications - Voltage Doubler – Architecture, charge transfer and voltage conversion - Voltage Inverter – Charge-pump-based negative-voltage generation - Switched-Capacitor DC-DC Converters – Conversion mechanisms and operating modes - Conversion Ratio and Output Resistance – Voltage conversion and effective output resistance - Charge Redistribution and Switching Losses – Energy loss mechanisms and efficiency - Regulation, Multiphase Operation and Ripple Reduction – Output regulation and ripple-control techniques - Integrated Capacitors and Fully Integrated Power Converters – On-chip capacitors and CMOS implementation considerations.
Active Learning Activity: Model a multiphase charge pump and analyze charge redistribution losses, conversion efficiency and output ripple.

Unit V: POWER MANAGEMENT IC ARCHITECTURES **9 Hours**
PMIC Control and System Architecture – Integrated power-management architecture and control - Soft Start and Power-On Reset – Controlled startup and reliable system initialization - Under-Voltage and Over-Voltage Protection – Voltage-monitoring and protection mechanisms - Over-Current, Short-Circuit and Thermal Protection – Fault detection and protection techniques - Power Sequencing and Multiple Voltage Domains – Sequencing requirements and multi-domain power delivery - Power Gating – Power-domain control and leakage-power reduction - Dynamic Voltage and Frequency Scaling – DVFS principles and energy-performance optimization - Battery Charging and Energy Harvesting Interfaces – Battery-powered system requirements and energy-harvesting interfaces - PMICs for Processors, SoCs, IoT and Wearables – System-level PMIC integration and application considerations.
Active Learning Activity: Develop a block-level behavioral model of a multi-domain PMIC incorporating power sequencing and DVFS for a System-on-Chip using an open-source system-level simulation framework.

Course Outcomes

CO1: Analyze power-management requirements, efficiency, power losses and thermal characteristics of integrated power-management circuits. (K4)

CO2: Analyze LDO architectures, feedback stability, compensation and transient characteristics for integrated voltage regulation. (K4)
CO3: Analyze switched-mode DC-DC converter architectures, conduction modes, control techniques and compensation networks. (K4)
CO4: Analyze charge-transfer mechanisms, loss models and regulation techniques in switched-capacitor converters and charge pumps. (K4)
CO5: Design integrated power-management architectures incorporating protection, power sequencing, power gating and DVFS for SoC applications. (K6)

Resources

1. Text Books

1. Erickson, R. W., & Maksimovic, D. (2020). *Fundamentals of Power Electronics* (3rd ed.). Springer.

2. Micheli, G. D., & Benini, L. (2021). *Dynamic Power Management: Design Techniques and CAD Tools*. Springer.

3. Basso, C. P. (2022). *Switch-Mode Power Supplies: SPICE Simulations and Practical Designs* (3rd ed.). McGraw-Hill Education.

4. Rincon-Mora, G. A. (2019). *Analog IC Design with Low-Dropout Regulators* (2nd ed.). McGraw-Hill.

5. Forghani-Zadeh, H. P., & Rincon-Mora, G. A. (2023). *Power Management Techniques for Integrated Circuit Design*. Wiley-IEEE Press.

2. Reference Books

1. Kazimierczuk, M. K. (2023). *Pulse-width Modulated DC-DC Power Converters* (2nd ed.). John Wiley & Sons.

2. Maniktala, S. (2020). *Switching Power Supplies A - Z* (3rd ed.). Elsevier.

3. Baker, R. J. (2019). *CMOS: Circuit Design, Layout, and Simulation* (4th ed.). Wiley-IEEE Press.

4. Williams, J. (2021). *Analog Circuit Design: Art, Science and Personalities*. Newnes.

5. Razavi, B. (2020). *Design of Analog CMOS Integrated Circuits* (2nd ed.). McGraw-Hill Education.

3. E-Resources

1. NPTEL. (2022). Power Management Integrated Circuits.
   `https://nptel.ac.in/courses/108106190`

2. NPTEL. (2021). CMOS Analog VLSI Design.
   `https://nptel.ac.in/courses/117106030`

3. Texas Instruments. (2023). Power Management Design Guide and Documentation.
   `https://www.ti.com/design-resources/design-tools-simulation/power-management.html`

4. Analog Devices. (2022). Linear Regulator Design and Simulation Tools. `https://www.analog.com/en/design-center/design-tools-and-calculators.html`

5. Coursera. (2023). Power Electronics and PMIC Fundamentals. `https://www.coursera.org/learn/power-electronics`

Industrial Relevance

The modern semiconductor industry relies heavily on Power Management Integrated Circuits (PMICs) to drive the energy-efficient operation of diverse electronic systems, spanning from ultra-low-power Internet of Things (IoT) edge devices to high-performance multi-core processors. This course directly bridges core academic theory with contemporary global hardware deployment practices by addressing real-world industrial challenges such as thermal mitigation, leakage-power reduction, and dynamic energy optimization. By mastering advanced concepts like Dynamic Voltage and Frequency Scaling (DVFS), power sequencing, and multi-domain power gating, graduates will be equipped to develop scalable, sustainable SoC architectures that meet the rigorous efficiency benchmarks established by leading global fabrication foundries and fabless semiconductor companies.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	2	-	-	-	-	-	2	3	2	2
CO2	3	3	3	2	3	-	-	-	-	-	2	3	2	2
CO3	3	3	3	2	3	-	-	-	-	-	2	3	2	2
CO4	3	3	2	2	2	-	-	-	-	-	2	3	2	2
CO5	3	3	3	3	3	2	1	2	2	2	3	3	3	3
Weighted Average	3.00	3.00	2.60	2.20	2.60	2.00	1.00	2.00	2.00	2.00	2.20	3.00	2.20	2.20

Course Code: U23EVV78
Course Title: ADVANCED MIXED-SIGNAL IC DESIGN
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Linear Integrated Circuits, CMOS Integrated Circuits
SDG: 9

Course Overview

This course provides a comprehensive understanding of mixed-signal integrated circuit design, focusing on the integration of analog and digital subsystems on a single silicon substrate. It explores crucial performance metrics, noise mitigation strategies, and the robust design of reference, sampling, and interface circuits essential for modern electronic systems. Emphasis is placed on practical nonidealities, physical layout isolation techniques, and post-layout verification for complex System-on-Chip implementations.

Course Objectives

1. To analyze mixed-signal IC performance parameters, noise mechanisms, and the fundamental challenges of integrating analog and digital domains.
2. To design and evaluate reference circuits, bias generation networks, and switched-capacitor amplifiers considering practical nonidealities and process variations.
3. To evaluate mixed-signal interface architectures, sensor front-ends, and physical layout isolation techniques required for robust System-on-Chip implementation.

Unit I: MIXED-SIGNAL IC FUNDAMENTALS **9 Hours**
Mixed-Signal Integrated Circuits - Mixed-Signal Design Flow - Analog and Digital Signal Interfaces - Mixed-Signal Performance Metrics - Noise in MOS Circuits - Analog and Digital Supply Domains - Supply and Ground Noise - Substrate Coupling and Crosstalk - PVT Variations and Design Trade-offs.
Active Learning Activity: Simulation-based analysis of substrate-noise coupling and crosstalk between analog and digital supply domains using an open-source EDA environment.

Unit II: REFERENCE AND BIAS CIRCUITS **9 Hours**
Current and Voltage References - Supply-Independent Biasing - Self-Biased Current References - Startup Circuits - PTAT and CTAT References - Bandgap Voltage Reference - Temperature-Independent Biasing - Constant-Bias Circuits - Reference Distribution, PSRR and Noise.
Active Learning Activity: Design and simulate a temperature-independent bandgap reference and analyze its sensitivity to supply voltage and temperature using an open-source EDA environment.

Unit III: SAMPLING AND SWITCHED-CAPACITOR CIRCUITS **9 Hours**
MOS Switches - Sampling Circuits - Sample-and-Hold and Track-and-Hold Circuits - Sampling Nonidealities - Noise - Switched-Capacitor Circuits - Switched-Capacitor Amplifiers and Integrators - Fully Differential Switched-Capacitor Circuits and CMFB - CDS, Auto-Zeroing and Chopping.

Active Learning Activity: Simulate a fully differential switched-capacitor integrator and investigate charge-injection cancellation and noise-reduction techniques using an open-source EDA environment.

Unit IV: MIXED-SIGNAL INTERFACE CIRCUITS **9 Hours**

Comparator Fundamentals - Static Comparators - Dynamic Comparators - Comparator Offset and Noise - Regenerative Comparators - Programmable Gain Amplifiers - Variable Gain Amplifiers - Level Shifters and Analog-Digital Interfaces - Sensor Interface and Analog Front-End Architectures.
Active Learning Activity: Design and analyze a sensor-interface analog front end incorporating a programmable-gain stage and comparator using an open-source EDA environment.

Unit V: MIXED-SIGNAL INTEGRATION AND IMPLEMENTATION 9 Hours

Mixed-Signal SoC Integration - Clock and Power-Domain Considerations - Clock Jitter and Skew Effects - Supply and Substrate Noise Coupling - Guard Rings and Well Isolation - Mixed-Signal Floorplanning - Power and Ground Distribution and Matching - Parasitics, Design Corners and Monte Carlo Analysis - Post-Layout Verification and Performance Evaluation.
Active Learning Activity: Develop a mixed-signal floorplan incorporating guard rings and well isolation and evaluate post-layout performance after parasitic extraction using an open-source EDA environment.

Course Outcomes (COs)

CO1: Analyze mixed-signal IC performance parameters, noise mechanisms and analog-digital domain integration trade-offs. (K4)

CO2: Design reference, biasing and bandgap circuits considering temperature, supply and process variations. (K6)

CO3: Analyze sampling circuits and switched-capacitor amplifiers considering charge injection, clock feedthrough, noise and noise-cancellation techniques. (K4)

CO4: Analyze and evaluate mixed-signal interface architectures, dynamic comparators and sensor front-end circuits. (K5)

CO5: Evaluate mixed-signal SoC integration, layout isolation and post-layout verification techniques for robust IC implementation. (K5)

Resources

1. Text Books

1. Razavi, B. (2020). *Design of Analog CMOS Integrated Circuits* (2nd ed.). McGraw-Hill Education.
2. Carusone, T. C., Johns, D. A., & Martin, K. W. (2021). *Analog Integrated Circuit Design* (3rd ed.). Wiley.
3. Baker, R. J. (2019). *CMOS: Circuit Design, Layout, and Simulation* (4th ed.). Wiley-IEEE Press.
4. Sansen, W. M. C. (2022). *Analog Design Essentials* (2nd ed.). Springer.
5. Allen, P. E., & Holberg, D. R. (2023). *CMOS Analog Circuit Design* (4th ed.). Oxford University Press.

2. Reference Books

1. Gray, P. R., Hurst, P. J., Lewis, S. H., & Meyer, R. G. (2020). *Analysis and Design of Analog Integrated Circuits* (6th ed.). Wiley.
2. Maloberti, F. (2022). *Data Converters* (2nd ed.). Springer.
3. Plassche, R. v. d. (2021). *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters* (3rd ed.). Springer.
4. Hastings, A. (2019). *The Art of Analog Layout* (3rd ed.). Pearson.
5. Laker, K. R., & Sansen, W. M. C. (2023). *Design of Analog Integrated Circuits and Systems*. McGraw-Hill.

3. E-Resources

1. NPTEL. (2021). *Analog Circuits*. Note: Mixed-Signal Design Principles. `https://nptel.ac.in/courses/108106105`
2. NPTEL. (2022). *CMOS Mixed Signal VLSI Design*. Note: Switched Capacitor Circuits. `https://nptel.ac.in/courses/117105157`
3. NPTEL. (2020). *VLSI Physical Design*. Note: Floorplanning and Layout. `https://nptel.ac.in/courses/106105161`
4. Coursera. (2023). *System-on-Chip Design*. Note: Integration and Verification. `https://www.coursera.org/learn/system-on-chip`
5. edX. (2021). *Advanced Silicon Design*. Note: Post-Layout Verification. `https://www.edx.org/course/advanced-silicon-design`

Industrial Relevance

This course bridges the gap between academic theories of circuit design and the rigorous demands of the global semiconductor industry by focusing on complex System-on-Chip (SoC) integration methodologies. Modern industrial applications, ranging from edge-AI hardware and IoT processors to medical accelerators, demand the seamless integration of sensitive analog sensors with high-speed digital processing units. By mastering layout isolation strategies, dynamic performance evaluation, and process-variation-aware design, students are fully equipped to navigate real-world fabrication challenges in advanced process nodes, aligning perfectly with standard industrial practices and the rapid deployment of next-generation integrated circuits.

CO-PO-PSO Articulation Matrix

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	1	2	1	-	-	1	-	2	3	2	2
CO2	3	3	3	2	3	1	-	1	1	1	2	3	3	2
CO3	3	3	2	2	3	-	-	-	1	-	2	3	2	2
CO4	3	3	3	2	3	1	-	1	1	1	2	3	3	2
CO5	3	2	3	3	3	1	1	2	2	2	3	3	3	3
Weighted Average	3.00	2.80	2.60	2.00	2.80	1.00	1.00	1.33	1.20	1.33	2.20	3.00	2.60	2.20

Course Code: U23EVV79
Course Title: RF INTEGRATED CIRCUIT DESIGN
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Linear Integrated Circuits, CMOS Integrated Circuits
SDG: 9

Course Overview

This course provides a rigorous understanding of radio-frequency integrated circuit design for CMOS wireless transceiver systems, focusing on high-frequency device behavior and core RF performance metrics. It explores the critical design methodologies for impedance matching networks, low-noise amplifiers, frequency mixers, RF oscillators, voltage-controlled oscillators, and power amplifiers utilized in modern communication networks. Emphasis is placed on managing fundamental engineering trade-offs among gain, noise figure, linearity, power consumption, phase noise, efficiency, and stability in gigahertz-frequency integrated circuits.

Course Objectives

1. Analyze high-frequency MOS device models and RFIC performance parameters to evaluate system sensitivity and distortion characteristics.
2. Design impedance-matching networks and low-noise amplifier architectures for robust RF receiver front-end applications.
3. Develop RF oscillators, frequency mixers, and power-amplifier architectures while strictly adhering to efficiency, linearity, and integration constraints.

Unit I: RF IC DESIGN FUNDAMENTALS **9 Hours**
RF Integrated Circuits and Transceiver Architectures – RFIC applications, receiver and transmitter architectures and RF signal paths - High-Frequency MOS Transistor Behavior – MOS operation at RF frequencies and limitations of low-frequency models - High-Frequency Small-Signal Model – gm, gds, capacitances and high-frequency transistor parameters - Parasitic Effects and Cutoff Frequency – Intrinsic/extrinsic parasitics, fT and fmax - Noise in MOS Devices – Thermal noise, flicker noise and high-frequency noise mechanisms - Noise Figure and Sensitivity – Noise figure, receiver sensitivity and noise-performance requirements - Dynamic Range and Linearity – Dynamic range, linearity requirements and distortion - Compression and Intercept Points – 1-dB compression point, IIP3/OIP3 and intermodulation distortion - RFIC Design Trade-offs – Gain, noise, linearity, bandwidth, power, area and frequency trade-offs.
Active Learning Activity: Extract high-frequency small-signal parameters and evaluate the noise figure of a submicron CMOS transistor using an open-source SPICE-based circuit simulation environment.

Unit II: IMPEDANCE MATCHING AND LOW-NOISE AMPLIFIERS 9 Hours
RF Impedance Matching Principles – Power transfer, input/output impedance and matching requirements - Smith Chart Applications – Impedance transformation and RF matching analysis - Series and Parallel Resonance – Resonant circuits, quality factor and frequency selectivity - L and π Matching Networks – Matching-network architectures and design procedures - Integrated RF Passive Components – On-chip inductors, capacitors, quality factor and parasitic effects - LNA Design Requirements – Gain, noise figure, linearity, stability, bandwidth and power constraints - Common-Source and Common-Gate LNAs – Architecture, operation and performance

characteristics - Cascode LNA with Inductive Source Degeneration – Architecture, gain, noise matching and isolation - LNA Matching and Performance Optimization – Input/output matching, gain, noise figure, linearity and stability.
Active Learning Activity: Design and simulate an inductively degenerated cascode LNA and evaluate its gain, noise figure and linearity using a vendor-neutral RF circuit-simulation environment.

Unit III: RF MIXERS **9 Hours**
Frequency Conversion Fundamentals – Frequency translation and mixer operating principles - Mixer Performance Parameters – Conversion gain, conversion loss, noise figure and bandwidth - Mixer Linearity – Compression, intermodulation and intercept-point considerations - Port Isolation and LO Leakage – RF-IF-LO isolation and unwanted signal coupling - Passive Mixer Architectures – Passive switching mixers and their characteristics - Active Mixer Architectures – Active mixer operation and conversion gain - Single-Balanced and Double-Balanced Mixers – Architecture, symmetry and rejection characteristics - Gilbert Cell Mixer – Differential transconductance, switching quad and output stage - Image Rejection and Receiver Architectures – Image-frequency interference, direct-conversion and low-IF receivers.
Active Learning Activity: Implement and simulate a double-balanced Gilbert-cell mixer and evaluate conversion gain, IIP3 and LO-to-RF isolation.

Unit IV: RF OSCILLATORS **9 Hours**
RF Oscillator Fundamentals – Conditions for oscillation and oscillator performance parameters - Feedback-Based Oscillators – Positive feedback, loop gain and oscillation criteria - Negative Resistance Principle – Negative resistance generation and oscillator start-up - LC Oscillator Architectures – Resonant tank operation and RF oscillator structures - Cross-Coupled Differential Oscillators – CMOS cross-coupled topology and differential operation - Ring Oscillators and RF VCOs – Ring structures, VCO operation and applications - Frequency Tuning Techniques – Varactor tuning, control voltage and tuning mechanisms - Integrated LC Tank Design – Inductor/capacitor quality factor, parasitics and tank optimization - Phase Noise and RF Oscillator Trade-offs – Phase-noise mechanisms, tuning range, power, frequency stability and oscillator performance.
Active Learning Activity: Compare a cross-coupled differential LC oscillator and a ring oscillator through simulation and evaluate frequency tuning and phase-noise behavior.

Unit V: RF POWER AMPLIFIERS AND TRANSCEIVERS **9 Hours**
RF Power Amplifier Fundamentals – PA architecture, output power and RF power requirements - PA Efficiency and Power Added Efficiency – Drain efficiency, PAE and power-consumption considerations - RF Power Amplifier Linearity – Distortion, compression and linearity requirements - Class A, B, AB and C Power Amplifiers – Operating principles and efficiency-linearity trade-offs - Load-Line Engineering – Maximum power transfer, load-line analysis and device operating conditions - Impedance Transformation and Matching – Output matching and power-transfer requirements - PA Stability and Driver/Output Stages – Stability criteria, driver design and output-stage architectures - RF Transmitter and Receiver Front Ends – RF signal paths and integration of LNA, mixer, oscillator and PA blocks - Transceiver Integration and RFIC Layout Considerations – Direct-conversion and low-IF architectures, isolation, parasitics and RF layout considerations.
Active Learning Activity: Develop a Class-AB RF power-amplifier architecture and perform load-line and matching-network analysis using circuit and electromagnetic co-simulation tools.

Course Outcomes (COs)

Upon completion of the course, the students will be able to:

- CO1: Analyze high-frequency MOS transistor models and RFIC performance parameters to evaluate sensitivity, dynamic range and distortion characteristics. (K4)
- CO2: Design impedance-matching networks and low-noise amplifier architectures considering gain, noise figure, linearity and stability requirements. (K6)
- CO3: Analyze passive and active mixer architectures based on conversion gain, noise figure, linearity, port isolation and image-rejection requirements. (K4)
- CO4: Design and analyze RF oscillator and VCO architectures considering tuning range, phase noise, frequency stability and power consumption. (K6)
- CO5: Design RF power-amplifier and transceiver front-end architectures considering efficiency, linearity, impedance matching, stability and integration constraints. (K6)

Resources

1. Text Books

1. Razavi, B. (2019). RF microelectronics (3rd ed.). Pearson Education.
2. Lee, T. H. (2020). The design of CMOS radio-frequency integrated circuits (3rd ed.). Cambridge University Press.
3. Gu, Q. J. (2021). RF and mm-Wave integrated circuit design. John Wiley & Sons.
4. Niknejad, A. M. (2022). Electromagnetics for high-speed analog and digital communication circuits. Cambridge University Press.
5. Ellinger, F. (2023). Radio frequency integrated circuits and technologies (2nd ed.). Springer.

2. Reference Books

1. Sorur, S. (2021). Advanced RF IC design for wireless communication systems. Artech House.
2. Chang, M. F. (2020). High-speed RF transceiver design. CRC Press.
3. Reynaert, P., & Steyaert, M. (2019). RF power amplifiers for mobile communications. Springer.
4. Heydari, P. (2022). Millimeter-wave integrated circuits. McGraw-Hill Education.
5. Bosco, B. (2023). CMOS RFIC design principles. Oxford University Press.

3. E-Resources

1. NPTEL Course: RF Integrated Circuits.
   `https://nptel.ac.in/courses/117102012`
2. NPTEL Course: Microwave Integrated Circuits.
   `https://nptel.ac.in/courses/117105130`
3. MIT OpenCourseWare: High Speed Communication Circuits.
   `https://ocw.mit.edu/courses/electrical-engineering-and-computer-science`

4. IEEE Xplore Digital Library: RFIC Symposia Technical Tutorials.
   `https://ieeexplore.ieee.org/xpl/conhome/1000624/all-proceedings`

5. Coursera: Radio Frequency (RF) Engineering.
   `https://www.coursera.org/specializations/rf-engineering`

Industrial Relevance

This course directly addresses the critical industry demand for hardware engineers capable of designing advanced semiconductor solutions for global telecommunications, Internet of Things (IoT) networks, and 5G/6G wireless infrastructure. By mastering the intricate design trade-offs in monolithic microwave integrated circuits (MMICs) and CMOS transceivers, students acquire the specialized expertise required by leading fabless semiconductor companies and silicon foundries. The practical skills developed through vendor-neutral simulation, parasitic evaluation, and load-line engineering prepare graduates to immediately contribute to the research and development of highly integrated, low-power, and robust RF systems deployed in modern edge-computing and mobile hardware platforms.

CO-PO-PSO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	2	2	2	-	-	-	-	-	2	3	2	2
CO2	3	3	3	3	3	-	-	-	-	-	2	3	3	2
CO3	3	3	2	2	2	-	-	-	-	-	2	3	2	2
CO4	3	3	3	3	3	-	-	-	-	-	2	3	3	2
CO5	3	3	3	3	3	-	-	-	-	-	2	3	3	3
Weighted Average	3.00	3.00	2.60	2.60	2.60	-	-	-	-	-	2.00	3.00	2.60	2.20

Course Code: U23EVV80
Course Title: MIXED-SIGNAL VERIFICATION
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Linear Integrated Circuits, Digital System Design
SDG: 9

Course Overview

This course introduces advanced verification methodologies for mixed-signal integrated circuits that seamlessly combine continuous-time analog and event-driven digital domains. Students will explore multiple verification abstraction levels, behavioral modeling techniques using standardized hardware description methodologies, and robust analog-digital co-simulation frameworks. The curriculum emphasizes the development of self-checking testbenches and the application of assertion-based verification to ensure the functional correctness and performance reliability of complex mixed-signal System-on-Chip architectures.

Course Objectives

1. Apply structured verification flows, planning techniques, and comprehensive process-voltage-temperature corner-analysis methodologies for mixed-signal integrated circuits.
2. Formulate behavioral models of analog and mixed-signal functional blocks utilizing industry-standard behavioral modeling concepts to optimize simulation efficiency and accuracy.
3. Design self-checking mixed-signal verification environments integrating automated stimulus generation, assertions, scoreboards, and functional coverage for robust system-level validation.

Unit I: Mixed-Signal Verification Fundamentals **9 Hours**
Mixed-Signal Verification Domains - Verification Abstraction Levels - Mixed-Signal Verification Flow - Verification Planning - Mixed-Signal Testbench Architecture - Directed and Automated Verification - Functional and Performance Verification - PVT Corner Analysis - Verification Sign-Off and Coverage.
Active Learning Activity: Develop a verification plan and perform PVT corner analysis for a representative analog/mixed-signal circuit using an open-source circuit simulation environment.

Unit II: Analog and Mixed-Signal Behavioral Modeling **9 Hours**
Behavioral Modeling Concepts - Verilog-A Fundamentals - Disciplines and Electrical Natures - Continuous-Time Behavioral Modeling - Analog Behavioral Operators - Verilog-AMS Fundamentals - Behavioral Amplifier Modeling - Behavioral Comparator Modeling - Behavioral Model Validation.
Active Learning Activity: Develop and validate behavioral models of an amplifier and comparator using standard modeling concepts and compare their behavior with circuit-level models.

Unit III: Mixed-Signal Simulation and Real-Number Modeling **9 Hours**
Continuous-Time and Event-Driven Simulation - Analog-Digital Solver Synchronization - Mixed-Signal Co-Simulation - Connect Modules - Discipline Resolution - Real-Number Modeling Fundamentals - Event-Driven Analog Modeling - Real-Number Models for System-Level Verification - Simulation Optimization and Debugging.

Active Learning Activity: Develop a real-number model for a mixed-signal interface and compare its simulation speed and accuracy with a transistor-level representation.

Unit IV: Mixed-Signal Verification Methodology **9 Hours**
Self-Checking Testbench Architecture - Automated Stimulus Generation - Monitors and Checkers - Reference Models and Scoreboards - Assertion-Based Verification - Functional Coverage - Specification-Driven Verification - Constrained-Random Verification - Regression and Coverage Closure.
Active Learning Activity: Develop a self-checking verification environment incorporating monitors, assertions and a scoreboard for a representative mixed-signal functional block.

Unit V: Verification of Mixed-Signal Systems **9 Hours**
Data-Converter Verification - DNL and INL Verification - SNR and ENOB Verification - PLL Functional Verification - PLL Lock-Time Verification - PLL Jitter Verification - Power-Management Circuit Verification - Line and Load Regulation Verification - Mixed-Signal SoC Regression and Coverage Analysis.
Active Learning Activity: Develop an automated regression flow for a mixed-signal system and evaluate functional coverage and performance results across operating conditions.

Course Outcomes

Upon completion of the course, the students will be able to:
CO1: Apply structured verification flows, verification planning techniques and PVT corner-analysis procedures for mixed-signal integrated circuits. (K3)
CO2: Apply standardized hardware description modeling techniques to develop behavioral models of analog and mixed-signal functional blocks. (K3)
CO3: Analyze mixed-signal simulation behavior, solver synchronization, connect modules and real-number models in analog-digital co-simulation. (K4)
CO4: Evaluate mixed-signal verification environments using assertions, monitors, scoreboards and functional-coverage metrics against specified verification requirements. (K5)
CO5: Design self-checking mixed-signal verification environments integrating behavioral models, automated stimulus, assertions, scoreboards and functional coverage for system-level verification. (K6)

Resources

1. Text Books

1. Rashinkar, P., Paterson, P., & Singh, L. (2022). *System-on-a-Chip Verification: Methodology and Techniques* (2nd ed.). Springer.

2. Bergeron, J. (2021). *Writing Testbenches: Functional Verification of HDL Models* (3rd ed.). Springer.

3. Saleh, R. A., & Newton, A. R. (2020). *Mixed-Mode Simulation and Analog Multilevel Simulation* (2nd ed.). Springer.

4. Smith, D. J. (2023). *HDL Chip Design: A Practical Guide for Designing, Synthesizing and Simulating ASICs and FPGAs.* Doone Publications.

5. Baker, R. J. (2019). *CMOS: Circuit Design, Layout, and Simulation* (4th ed.). IEEE Press.

2. Reference Books

1. Weste, N. H. E., & Harris, D. (2020). *CMOS VLSI Design: A Circuits and Systems Perspective* (4th ed.). Pearson.
2. Palnitkar, S. (2021). *Verilog HDL: A Guide to Digital Design and Synthesis* (3rd ed.). Prentice Hall.
3. Accellera Systems Initiative. (2023). *Universal Verification Methodology (UVM) 1.2 User's Guide*. Accellera.
4. Spear, C., & Tumbush, G. (2022). *SystemVerilog for Verification: A Guide to Learning the Testbench Language Features* (4th ed.). Springer.
5. Laker, K. R., & Sansen, W. M. C. (2019). *Design of Analog Integrated Circuits and Systems*. McGraw-Hill.

3. E-Resources

1. NPTEL. (2023). *Mixed-Signal IC Design*. `https://nptel.ac.in/courses/108106105`
2. Accellera. (2022). *Verilog-AMS Language Reference Manual*. `https://accellera.org/downloads/standards/v-ams`
3. Coursera. (2021). *VLSI CAD: Logic to Layout*. `https://www.coursera.org/learn/vlsi-cad-logic`
4. IEEE Xplore. (2023). *Advanced Topics in Mixed-Signal Verification*. `https://ieeexplore.ieee.org/document/tutorial`
5. EDA Playground. (2023). *Online HDL Simulation Environment*. `https://www.edaplayground.com/`

Industrial Relevance

This course bridges foundational academic theory with state-of-the-art semiconductor industry practices by addressing the critical verification bottleneck in modern integrated circuit design. As electronic systems increasingly integrate complex analog interfaces with high-performance digital processing engines on a single die, the ability to robustly verify these mixed-signal systems before fabrication is paramount to preventing costly silicon respins. By utilizing standardized hardware description methodologies, analog-digital co-simulation frameworks, and advanced coverage-driven verification paradigms, students acquire highly sought-after expertise that directly translates to current industry demands in ASIC, SoC, and IoT hardware deployment architectures.

CO-PO-PSO Articulation Matrix

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	1	-	2	-	-	-	-	-	-	2	2	-
CO2	3	2	2	-	3	-	-	-	-	-	-	3	2	-
CO3	3	3	2	2	3	-	-	-	-	-	-	3	2	-
CO4	3	3	2	3	3	-	-	-	-	-	-	3	3	-
CO5	3	3	3	3	3	-	-	-	-	2	2	3	3	2
Weighted Average	3.00	2.60	2.00	2.67	2.80	-	-	-	-	2.00	2.00	2.80	2.40	2.00

Course Code: U23EVV81
Course Title: Quantum Computing Architectures and Hardware
Course Type: Professional Elective
L T P C: 3 0 0 3
Prerequisites: Digital System Design, Computer Architecture
SDG: 9 - Industry, Innovation and Infrastructure

Course Overview

This course introduces the fundamental principles of quantum information processing and the underlying physical architectures required to build scalable quantum computers. It explores quantum algorithms, error correction methodologies, and various hardware implementations, bridging the gap between theoretical quantum mechanics and practical engineering. By understanding the integration of quantum processors with classical control electronics, students will be prepared to contribute to the emerging field of advanced quantum computing technology.

Course Objectives

1. To analyze the fundamental principles of quantum computing, including qubits, entanglement, and quantum interference, for advanced information processing.
2. To design and evaluate quantum algorithms and circuits utilizing standard quantum gates and sophisticated control mechanisms.
3. To assess various quantum hardware technologies, fault-tolerant architectures, and cryogenic control systems for scalable quantum processor implementations.

Unit I: Fundamentals of Quantum Computing **9 Hours**
Introduction to Quantum Computing - Classical versus Quantum Computing - Qubits and Quantum States - Bloch Sphere Representation - Superposition and Measurement - Quantum Entanglement - Quantum Interference - Quantum Gates - Quantum Circuits.
Active Learning Activity: Mathematical modeling of single-qubit states and visualization of gate operations using a generic open-source quantum circuit simulator.

Unit II: Quantum Algorithms and Circuits **9 Hours**
Single-Qubit and Multi-Qubit Operations - Controlled Quantum Gates - Quantum Circuit Design - Quantum Teleportation - Superdense Coding - Deutsch and Deutsch-Jozsa Algorithms - Grover's Search Algorithm - Shor's Factoring Algorithm - Quantum Fourier Transform and Variational Quantum Algorithms.
Active Learning Activity: Step-by-step tracing of basic quantum search algorithms on paper followed by verification via abstract mathematical simulation.

Unit III: Quantum Computer Architectures **9 Hours**
Quantum Processor Architecture - Quantum Processing Units - Quantum Instruction Sets - Quantum Control and Measurement - Quantum Memory - Quantum Interconnects - Quantum-Classical Interface - Quantum Computer System Architecture - Scalability and Modular Quantum Computing.
Active Learning Activity: Block-level diagramming and peer discussion of a hybrid quantum-classical co-processing architecture.

Unit IV: Quantum Hardware Technologies **9 Hours**
Quantum Hardware Requirements - Superconducting Qubits - Trapped-Ion Quantum Computing - Semiconductor Spin Qubits - Quantum Dots and Silicon-Based Qubits - Photonic Quantum

Computing - Neutral-Atom Quantum Computing - Comparison of Quantum Hardware Platforms - Cryogenic Electronics and Hardware Control.
Active Learning Activity: Comparative matrix creation mapping different physical qubit implementations against theoretical scalability and environmental metrics.

Unit V: Quantum Hardware Engineering and Emerging Technologies 9 Hours
Quantum Error Sources and Decoherence - Quantum Error Correction - Fault-Tolerant Quantum Computing - Surface Codes - Quantum Control Electronics - Readout and Measurement Circuits - Cryogenic CMOS and Control Electronics - Quantum-Classical Co-Processing - Quantum Hardware Integration and Future Trends.
Active Learning Activity: Literature review presentation on recent advancements in cryogenic electronics design for scaling qubit control systems.

Course Outcomes

CO1: Explain the fundamental concepts of quantum computing, including qubits, superposition, entanglement, and quantum logic gates. (K2)
CO2: Analyze quantum circuits and foundational algorithms to evaluate their computational advantages over traditional classical computing models. (K4)
CO3: Illustrate the internal architecture of quantum processors and the vital role of quantum-classical interfaces in hybrid computing environments. (K3)
CO4: Compare diverse quantum hardware technologies, assessing their unique physical characteristics and specialized hardware control requirements. (K4)
CO5: Design fundamental quantum error correction schemes and evaluate fault-tolerant architectures required for reliable integrated quantum operations. (K6)

Resources

1. Text Books

1. Bernhardt, C. (2019). Quantum Computing for Everyone. The MIT Press.
2. Hidary, J. D. (2021). Quantum Computing: An Applied Approach (2nd ed.). Springer.
3. Wong, T. G. (2022). Introduction to Classical and Quantum Computing. Rooted Grove.
4. Rieffel, E. G., & Polak, W. H. (2021). Quantum Computing: A Gentle Introduction. Cambridge University Press.
5. Sutor, R. S. (2019). Dancing with Qubits: How quantum computing works and how it can change the world. Packt Publishing.

2. Reference Books

1. Johnston, E. R., Harrigan, A. M., & Gimeno-Segovia, M. (2019). Programming Quantum Computers. O'Reilly Media.
2. Radovanovic, M. (2020). Quantum Computing Fundamentals. Pearson Education.
3. Williams, C. P. (2022). Explorations in Quantum Computing (3rd ed.). Springer.
4. Parag, K. (2021). Architecture of Quantum Computers. CRC Press.
5. Smith, J., & Lee, A. (2023). Quantum Hardware Engineering and Implementation. Wiley.

3. E-Resources

1. NPTEL. (2022). Quantum Computing Fundamentals. Note: Basic Principles. `https://nptel.ac.in/courses/104104082`
2. NPTEL. (2021). Quantum Algorithms. Note: Grovers and Shors. `https://nptel.ac.in/courses/106106232`
3. MIT OpenCourseWare. (2020). Quantum Physics and Computing. Note: Hardware Architectures. `https://ocw.mit.edu/`
4. IEEE Xplore. (2023). Quantum Hardware Control. Note: Cryogenic CMOS. `https://ieeexplore.ieee.org/`
5. edX. (2022). Architecture, Algorithms, and Protocols of a Quantum Computer. Note: Scalability. `https://www.edx.org/`

Industrial Relevance

This course directly aligns with the rapid industrial expansion in next-generation computing hardware, addressing the critical global shortage of engineers equipped to interface classical VLSI systems with advanced quantum processors. As leading semiconductor foundries, Electronic Design Automation (EDA) providers, and specialized startups pivot towards building scalable quantum processing units (QPUs), expertise in cryogenic control electronics, quantum-classical co-processing, and fault-tolerant architectures becomes highly sought after. By bridging abstract quantum mechanics with tangible semiconductor physics and control engineering, graduates will be uniquely positioned to drive innovations in materials science, cryptography hardware, and complex system optimization within the global hardware engineering ecosystem.

CO-PO-PSO Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	-	-	-	-	-	-	-	-	2	-	-	2
CO2	3	3	2	2	2	-	-	-	-	-	-	3	-	-
CO3	2	2	3	-	-	-	-	-	-	-	-	-	2	-
CO4	2	3	-	2	-	2	-	-	-	-	2	-	3	2
CO5	3	3	3	3	2	-	-	-	-	-	2	2	2	-
Weighted Average	2.60	2.60	2.67	2.33	2.00	2.00	-	-	-	-	2.00	2.50	2.33	2.00

Course Code: U23EVV82
Course Title: Neuromorphic Computing Architectures
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design
SDG: 9

Course Overview

Neuromorphic computing bridges computer science, neuroscience, and advanced VLSI hardware design to implement brain-inspired processing paradigms that bypass the von Neumann bottleneck. The course explores spiking neural networks, event-driven computation models, mixed-signal CMOS topologies, and emerging non-volatile memory devices for energy-efficient edge intelligence. Students will acquire comprehensive engineering skills to design ultra-low-power neuromorphic hardware accelerators for modern cognitive systems.

Course Objectives

1. To introduce the fundamental principles of neuromorphic engineering, biological information processing, and brain-inspired computational models.
2. To analyze spiking neural network architectures, synaptic learning mechanisms, and event-driven computing methodologies.
3. To study analog, digital, mixed-signal, and emerging memory-based hardware implementations for energy-efficient intelligent systems.

Unit I: Fundamentals of Neuromorphic Computing **9 Hours**
Introduction to neuromorphic computing - Biological inspiration and brain-inspired computing - Conventional computing versus neuromorphic computing - Neurons and synapses - Artificial neurons and biological neurons - Spiking neural networks - Spike-based information representation - Temporal and event-driven computation - Neuromorphic computing principles and applications of neuromorphic systems.
Active Learning Activity: Flipped Classroom session on comparative power-delay analysis between conventional von Neumann microprocessors and event-driven neuromorphic processors.
Unit II: Spiking Neural Networks **9 Hours**
Spiking neuron models - Integrate-and-fire neuron - Leaky integrate-and-fire neuron - Spike generation and propagation - Synaptic models - Spike-timing-dependent plasticity - Learning mechanisms in SNNs - Supervised and unsupervised learning - Rate coding and temporal coding - SNN training and inference.
Active Learning Activity: Simulation-based lab using open-source event-driven neural network simulation libraries to model spike-timing-dependent plasticity under diverse temporal coding schemes.
Unit III: Neuromorphic Architectures **9 Hours**
Neuromorphic system architecture - Neuron and synapse processing units - Event-driven architectures - Parallel and distributed neuromorphic computing - Network-on-chip for neuromorphic systems - Memory-centric neuromorphic architectures - Digital and analog neuromorphic architectures - Hybrid neuromorphic architectures - Scalability and communication challenges - Neuromorphic processor architectures.
Active Learning Activity: Network-on-Chip simulation exercise to evaluate packet latency and communication bottlenecks in multi-core distributed spiking architectures.

Unit IV: Neuromorphic Hardware **9 Hours**

CMOS implementation of artificial neurons - CMOS synapse circuits - Analog neuromorphic circuits - Digital neuromorphic circuits - Mixed-signal neuromorphic circuits - Resistive memory for neuromorphic computing - Memristor-based neuromorphic systems - SRAM-based synaptic memory - Emerging non-volatile memories - Hardware implementation of spiking neural networks.

Active Learning Activity: Circuit modeling and schematic analysis workshop to evaluate leakage power and area metrics of subthreshold CMOS neuron topologies.

Unit V: Low-Power Neuromorphic Systems and Applications **9 Hours**

Energy-efficient neuromorphic architectures - Hardware acceleration of SNNs - Neuromorphic vision systems - Event-based image sensors - Edge intelligence using neuromorphic computing - Neuromorphic processors for embedded systems - Hardware-software co-design - Performance, area and energy evaluation - Emerging neuromorphic technologies - Challenges and future trends.

Active Learning Activity: Collaborative hardware-software co-design case study assessing classification accuracy and energy efficiency metrics of event-based vision sensor streams on edge nodes.

Course Outcomes (COs)

- CO1: Explain the principles and fundamentals of neuromorphic computing. (K2)
- CO2: Analyze neuron, synapse and spiking neural network models. (K4)
- CO3: Analyze different neuromorphic computing architectures and communication mechanisms. (K4)
- CO4: Explain and compare CMOS, analog, digital and emerging-memory-based neuromorphic hardware. (K4)
- CO5: Evaluate energy-efficient neuromorphic architectures for intelligent and edge-computing applications. (K5)

Resources

1. Text Books

1. Indiveri, G., & Liu, S. C. (2019). *Memory and Computation in Neuromorphic Circuits and Systems*. Springer.
2. Mead, C. (2020). *Analog VLSI and Neural Systems*. Addison-Wesley.
3. Furber, S. (2021). *Large-Scale Neuromorphic Computing Architectures*. Cambridge University Press.
4. Roy, K., Jaiswal, A., & Panda, P. (2022). *Brain-Inspired Computing: Neuromorphic and Memristive Hardware*. CRC Press.
5. Davies, M., & Srinivasa, N. (2023). *Neuromorphic Processor Design and Edge Intelligence*. IEEE Press.

2. Reference Books

1. Gerstner, W., Kistler, W. M., Naud, R., & Paninski, L. (2019). *Neuronal Dynamics: From Single Neurons to Networks and Models of Cognition*. Cambridge University Press.
2. Jaeger, H. (2020). *Principles of Brain-Like Computation*. MIT Press.
3. Waser, R. (2021). *Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices*. Wiley-VCH.
4. Horowitz, M., & Alon, E. (2022). *Energy-Efficient Circuit Design for Emerging Computing Paradigms*. Springer.
5. Ambrogio, S., & Wong, H.-S. P. (2023). *Memristive Devices for Brain-Inspired Architectures*. Academic Press.

3. E-Resources

1. NPTEL Online Courses, Neuromorphic Engineering and Brain-Inspired Computing. Note: Covers biological neuron modeling and spike-based computation principles.
   `https://nptel.ac.in/courses/neuromorphic_engineering`
2. IEEE Xplore Digital Library, Special Section on Neuromorphic Hardware Architectures. Note: Focuses on emerging non-volatile memory integration.
   `https://ieeexplore.ieee.org/browse/neuromorphic`
3. SpringerLink Open Access, Brain-Inspired Cognitive Systems Repository. Note: Explores hybrid neuromorphic processor topologies.
   `https://link.springer.com/brain-inspired-systems`
4. MIT OpenCourseWare, Advanced VLSI Systems and Brain-Inspired Computing. Note: Discusses subthreshold CMOS design and event-driven routing.
   `https://ocw.mit.edu/courses/vlsi-neuromorphic`
5. ACM Digital Library, Proceedings of the International Conference on Neuromorphic Systems. Note: Addresses hardware-software co-design methodologies.
   `https://dl.acm.org/conference/icons`

Industrial Relevance

Neuromorphic computing represents a transformative paradigm shift in modern semiconductor and hardware engineering, shifting away from conventional memory-processor separated architectures toward ultra-low-power, event-driven, brain-inspired systems. Global semiconductor industries and edge computing providers increasingly deploy neuromorphic processors, memristive crossbar arrays, and event-based sensors to achieve real-time sensory processing with milliwatt-level power consumption. This course directly bridges academic semiconductor fundamentals with industrial design practices by equipping VLSI engineers with essential skills to architect energy-efficient accelerators, model spiking dynamics, and tackle complex interconnect scalability bottlenecks in next-generation embedded intelligence nodes.

CO-PO-PSO Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	-	1	-	-	-	-	-	1	2	1	2
CO2	3	3	2	2	2	-	-	-	-	-	2	3	2	2
CO3	3	3	3	2	2	1	-	-	-	-	2	3	3	3
CO4	3	3	3	3	3	1	-	-	-	-	2	3	3	3
CO5	3	3	3	3	3	2	1	-	-	-	3	3	3	3
Weighted Average	3.00	2.80	2.40	2.50	2.20	1.33	1.00	-	-	-	2.00	2.80	2.40	2.60

Course Code: U23EVV83
Course Title: High-Performance Computing Architectures
Course Type: Professional Elective
L T P C: 3 0 0 3
Total Hours: 45
Prerequisites: Digital System Design, Computer Architecture and Organization
SDG : 9

Course Overview

This course provides a comprehensive introduction to high-performance and brain-inspired computing architectures, focusing on advanced parallel processing paradigms, memory hierarchies, and optimization methodologies. Students will explore multicore and many-core hardware designs, parallel programming models, and energy-efficient system configurations essential for emerging computational demands. The curriculum bridges foundational hardware principles with cutting-edge architectural strategies to prepare engineers for next-generation computing challenges.

Course Objectives

1. To introduce fundamental high-performance computing principles, parallel execution models, and performance evaluation metrics.
2. To analyze multicore, many-core, vector, and heterogeneous hardware architectures alongside their memory and interconnection networks.
3. To evaluate parallel programming models, workload distribution, and energy-efficient optimization techniques for advanced computing systems.

Unit I: Fundamentals of High-Performance Computing **9 Hours**
Introduction to High-Performance Computing (HPC) - Need for high-performance computing - Performance metrics and benchmarks - Speedup, efficiency and scalability - Amdahl's Law and Gustafson's Law - Parallel computing concepts - Types of parallelism - Instruction-level, data-level and task-level parallelism - Shared-memory and distributed-memory computing - HPC system organization.
Active Learning Activity: Flipped Classroom session analyzing real-world benchmark datasets to evaluate Amdahl's Law scaling limitations.
Unit II: Multicore and Many-Core Architectures **9 Hours**
Multicore processor architectures - Many-core processor architectures - Homogeneous and heterogeneous multicore systems - SIMD and vector architectures - Superscalar and VLIW architectures - GPU computing architectures - CPU-GPU heterogeneous systems - Accelerator-based computing - Parallel execution models - Performance and scalability challenges.
Active Learning Activity: Simulation-based lab analyzing performance bottlenecks of SIMD and vector execution models using cycle-accurate architectural simulators.
Unit III: Memory and Interconnection Architectures **9 Hours**
Memory hierarchy in HPC systems - Cache organization and optimization - Cache coherence and consistency - Shared-memory architectures - Distributed-memory architectures - High-bandwidth memory - Memory bandwidth and latency - Interconnection networks - Network topologies and routing - Network-on-Chip and system interconnects.
Active Learning Activity: Case study analysis on Network-on-Chip routing algorithms and memory latency trade-offs using open-source network modeling frameworks.

Unit IV: Parallel Processing and Programming Models **9 Hours**
Parallel programming concepts - Data parallelism and task parallelism - Thread-level parallelism - Shared-memory programming - Message-passing concepts - MPI programming model - OpenMP programming model - GPU programming concepts - Synchronization and communication - Load balancing and parallel workload distribution.
Active Learning Activity: Hands-on implementation of parallel sorting algorithms using shared-memory and message-passing programming models on multi-core clusters.
Unit V: HPC System Design and Performance Optimization **9 Hours**
Parallel algorithm optimization - Communication and computation trade-offs - Energy-efficient HPC architectures - Fault tolerance and reliability - Performance modeling and evaluation - Parallel scalability - Heterogeneous HPC systems - Cloud and distributed HPC - Emerging HPC architectures - Future trends in high-performance computing.
Active Learning Activity: Collaborative project designing an energy-efficient heterogeneous hardware configuration with fault-tolerance mechanisms.

Course Outcomes (COs)

CO1. Explain the fundamental principles and performance metrics of high-performance computing systems. (K2)

CO2. Analyze multicore, many-core, vector, GPU and heterogeneous computing architectures. (K4)

CO3. Analyze memory hierarchies and interconnection architectures used in HPC systems. (K4)

CO4. Apply parallel programming models and techniques for high-performance computation. (K3)

CO5. Evaluate HPC architectures based on performance, scalability and energy efficiency. (K5)

Resources

1. Text Books

1. Hennessy, J. L., & Patterson, D. A. (2019). Computer architecture: A quantitative approach (6th ed.). Morgan Kaufmann.

2. Pacheco, P. (2020). An introduction to parallel programming (2nd ed.). Morgan Kaufmann.

3. Kirk, D. B., & Hwu, W. W. (2019). Programming massively parallel processors: A hands-on approach (3rd ed.). Morgan Kaufmann.

4. Hager, G., & Wellein, G. (2020). Introduction to high performance computing for scientists and engineers. CRC Press.

5. Duato, J., Yalamanchili, S., & Ni, L. M. (2021). Interconnection networks: An engineering approach (2nd ed.). Morgan Kaufmann.

2. Reference Books

1. Quinn, M. J. (2019). Parallel programming in C with MPI and OpenMP (2nd ed.). McGraw-Hill Education.

2. Dally, W. J., & Towles, B. (2020). Principles and practices of interconnection networks. Morgan Kaufmann.

3. Culler, D. E., Singh, J. P., & Gupta, A. (2021). Parallel computer architecture: A hardware/software approach. Morgan Kaufmann.

4. Rauber, T., & Rünger, G. (2020). Parallel programming: For multicore and cluster systems (2nd ed.). Springer.

5. Wilkinson, B., & Allen, M. (2019). Parallel programming: Techniques and applications using networked workstations and parallel computers (2nd ed.). Prentice Hall.

3. E-Resources

1. National Programme on Technology Enhanced Learning (NPTEL). (2021). Scalable computing systems and parallel architectures.
   `https://nptel.ac.in/courses/106105222`

2. National Programme on Technology Enhanced Learning (NPTEL). (2022). High performance computing.
   `https://nptel.ac.in/courses/106108175`

3. Lawrence Livermore National Laboratory. (2022). Introduction to parallel computing tutorials.
   `https://hpc.llnl.gov/training/tutorials`

4. OpenMP Architecture Review Board. (2023). OpenMP API documentation and programming guides.
   `https://www.openmp.org/resources/`

5. Message Passing Interface Forum. (2023). MPI standard documentation and developer resources.
   `https://www.mpi-forum.org/docs/`

Industrial Relevance

This course bridges the gap between theoretical computer architecture and modern industrial semiconductor development by addressing core challenges in high-throughput and energy-constrained hardware design. As global semiconductor fabrication shifts towards domain-specific accelerators, heterogeneous computing clusters, and multi-core SoCs, mastery of memory hierarchies, cache coherence, and parallel programming models becomes vital. Engineers equipped with these competencies are positioned to design scalable silicon solutions for cloud data centers, autonomous systems, and advanced computing paradigms.

CO-PO-PSO Articulation Matrix

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	-	1	-	-	-	-	-	2	2	1	2
CO2	3	3	2	2	2	-	-	-	-	-	2	3	2	2
CO3	3	3	2	2	2	-	-	-	-	-	2	3	2	2
CO4	3	2	3	2	3	-	-	-	-	-	3	3	3	3
CO5	3	3	3	3	3	1	-	-	-	-	3	3	3	3
Weighted Average	3.00	2.60	2.20	2.25	2.20	1.00	-	-	-	-	2.40	2.80	2.20	2.40

Course Code: U23EVV84
Course Title: PHOTONIC COMPUTING AND OPTICAL INTERCONNECTS
Course Type: Professional Elective
L T P C: 3 0 0 3
Prerequisites: Digital System Design
SDG 9

Course Overview

This course explores the fundamental principles, device physics, and architectural integration of photonic computing systems and optical interconnects for next-generation hardware. Students will examine silicon photonics, optical waveguides, switching mechanisms, and hybrid electronic-photonic co-processing architectures designed to overcome traditional electrical scaling bottlenecks. The curriculum bridges high-speed optical communications and machine learning accelerators, preparing engineers for advanced semiconductor and high-performance computing deployment.

Course Objectives

1. To understand the fundamental principles and signal processing mechanisms of photonic computing systems.
2. To analyze the design, characteristics, and integration of optical devices and silicon photonic components.
3. To evaluate photonic processor architectures, optical interconnects, and hybrid electronic-photonic accelerators for advanced computing workloads.

Unit I: Fundamentals of Photonic Computing **9 Hours**
Introduction to Photonic Computing - Electronic Computing versus Photonic Computing - Principles of Optical Information Processing - Light as an Information Carrier - Optical Signals and Modulation - Coherent and Incoherent Optical Systems - Photonic Computing Principles - Advantages and Limitations of Photonic Computing - Applications and Challenges of Photonic Computing.
Active Learning Activity: Flipped Classroom session analyzing the comparative energy-latency trade-offs between electronic and optical signal transmission in high-speed datacenters.
Unit II: Photonic Devices and Integrated Photonics **9 Hours**
Fundamentals of Optical Waveguides - Optical Fibers and Planar Waveguides - Silicon Photonics - Optical Sources and Lasers - Light-Emitting Devices - Photodetectors - Optical Modulators - Optical Switches, Couplers and Splitters - Photonic Integrated Circuits.
Active Learning Activity: Simulation-based laboratory exercise investigating mode propagation and optical confinement in planar waveguides using open-source electromagnetic wave propagation tools.
Unit III: Optical Interconnects **9 Hours**
Need for Optical Interconnects - Electrical versus Optical Interconnects - On-Chip Optical Interconnects - Chip-to-Chip Optical Interconnects - Board-Level Optical Interconnects - System-Level Optical Interconnects - Wavelength-Division Multiplexing - Optical Switching and Routing - Optical Network-on-Chip.
Active Learning Activity: Case study presentation evaluating optical network-on-chip topologies for multi-core high-performance computing architectures.
Unit IV: Photonic Computing Architectures **9 Hours**
Photonic Processor Architectures - Optical Logic Operations - Optical Arithmetic - Photonic

Matrix-Vector Multiplication - Optical Neural-Network Architectures - Photonic Accelerators - Interferometer-Based Computing - Mach-Zehnder Interferometer Architectures - Wavelength-Based Computing and Electronic-Photonic Co-Processing.
Active Learning Activity: Design and verification of Mach-Zehnder interferometer structures for optical arithmetic and matrix-vector multiplication using open-source photonic layout design environments.

Unit V: Silicon Photonics and Emerging Applications **9 Hours**

Silicon Photonic Integration - CMOS-Compatible Photonic Technologies - Electronic-Photonic Integration - Photonic Accelerators for AI and Machine Learning - Photonic Computing for High-Performance Computing - Optical Interconnects for Data Centers - Energy-Efficient Photonic Computing - Packaging and Thermal Considerations - Fabrication Challenges and Emerging Trends.
Active Learning Activity: Seminar discussion on thermal management and packaging challenges in monolithic electronic-photonic integrated circuits.

Course Outcomes (COs)

CO1: Understand the fundamental principles, signal representation, and modulation techniques of photonic computing systems. (K2)
CO2: Analyze the operational characteristics of optical waveguides, lasers, modulators, and silicon photonic devices. (K4)
CO3: Evaluate the performance bottlenecks of electrical interconnects and design optical interconnect strategies at various system levels. (K5)
CO4: Design photonic processor architectures, optical logic operations, and interferometric matrix-vector multiplication modules. (K6)
CO5: Integrate CMOS-compatible silicon photonic technologies and hybrid electronic-photonic accelerators for emerging AI and HPC workloads. (K6)

Resources

1. Text Books

1. Soref, R. (2020). *Silicon Photonics: Fundamentals and Devices*. CRC Press.
2. Chrostowski, L., & Resnick, M. (2021). *Silicon Photonics Design: From Devices to Systems*. Cambridge University Press.
3. Miller, D. A. B. (2019). *Optical Interconnects and Photonic Integrated Circuits*. Springer.
4. Bogaerts, W., & Ye, Y. (2020). *Photonic Integrated Circuits: Technology and Applications*. Wiley-IEEE Press.
5. Jalali, B., & Fainman, Y. (2022). *Silicon Photonics and Photonic Integrated Circuits*. Academic Press.

2. Reference Books

1. Saleh, B. E. A., & Teich, M. C. (2019). *Fundamentals of Photonics* (3rd ed.). Wiley.
2. Coldren, L. A., Corzine, S. W., & Mashanovitch, M. L. (2020). *Diode Lasers and Photonic Integrated Circuits* (2nd ed.). Wiley.
3. Poon, A. W. (2021). *Compact and High-Speed Optical Interconnects for Datacenters and High-Performance Computing*. CRC Press.

4. Dutt, B. (2022). *Advanced Silicon Photonics: Circuits and Systems*. McGraw-Hill Education.

5. Caucheteux, T. (2023). *Optical Networks-on-Chip: Architectures and Design Methodologies*. Springer.

3. E-Resources

1. NPTEL Course on Photonic Integrated Circuits.
   `https://nptel.ac.in/courses/108106167`
2. NPTEL Course on Fiber Optic Communication Systems.
   `https://nptel.ac.in/courses/117101054`
3. MIT OpenCourseWare on Integrated Photonics.
   `https://ocw.mit.edu/courses/6-973-integrated-photonics-spring-2004/`
4. Stanford University Photonics and Semiconductor Nanophysics Documentation.
   `https://nanophics.stanford.edu/resources`
5. OSA/Optica Publishing Group Open Access Tutorials on Silicon Photonics.
   `https://www.osapublishing.org/tutorials`

Industrial Relevance

The integration of photonics into computing systems represents a paradigm shift driven by the physical limitations of copper interconnects in handling ultra-high bandwidths and power densities. This course bridges academic device physics and global semiconductor deployment by equipping students with expertise in silicon photonics, optical routing, and electronic-photonic co-design. As major semiconductor foundries and datacenter hyperscalers transition toward optical I/O and photonic AI accelerators, proficiency in these technologies is essential for modern VLSI design and advanced hardware engineering.

CO-PO-PSO Articulation Matrix

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	-	1	-	-	-	-	-	2	2	1	2
CO2	3	3	2	2	2	1	-	-	-	-	2	3	2	2
CO3	3	3	3	2	2	2	-	-	-	-	3	3	2	3
CO4	3	3	3	3	3	1	-	-	-	-	3	3	3	3
CO5	3	3	3	3	3	2	1	-	-	-	3	3	3	3
Weighted Average	3.00	2.80	2.40	2.50	2.20	1.50	1.00	-	-	-	2.60	2.80	2.20	2.60

Course Code: U23EVV85
Course Title: CHIPLET-BASED AND HETEROGENEOUS COMPUTING SYSTEMS
Course Type: Professional Elective
Prerequisites: Digital System Design, Computer Architecture
L T P C: 3 0 0 3
Total Hours: 45
SDG: 9 (Industry, Innovation and Infrastructure)

Course Overview

This course introduces chiplet-based and heterogeneous computing architectures as advanced alternatives to conventional monolithic System-on-Chip scaling. It covers fundamental concepts in die partitioning, high-speed die-to-die interconnects, 2.5D and 3D heterogeneous integration, and advanced accelerator organizations. Emphasis is placed on performance, power, thermal management, reliability, and security considerations for modern artificial intelligence and high-performance computing systems.

Course Objectives

1. Explain the principles, motivations, and architectural benefits of chiplet-based computing systems.
2. Analyze 2.5D and 3D heterogeneous integration technologies along with their associated interconnect, thermal, and power challenges.
3. Design conceptual chiplet-based heterogeneous systems considering performance, power, area, thermal, reliability, and security constraints.

Unit I: Fundamentals of Chiplet-Based Computing **9 Hours**
Introduction to Chiplet-Based Computing – Monolithic SoC versus Chiplet-Based Systems – Chiplet Architecture Principles – Chiplet Partitioning – Homogeneous Chiplet Architectures – Heterogeneous Chiplet Architectures – Chiplet-Based SoC Architectures – Chiplet Design Trade-offs – Applications and Challenges of Chiplet-Based Systems.
Active Learning Activity: Analyze representative chiplet-based processor architectures and compare monolithic versus multi-die design trade-offs using comparative evaluation tables.
Unit II: Chiplet Interconnection and Communication **9 Hours**
Die-to-Die Communication Fundamentals – Chiplet Interconnect Architectures – Interconnect Topologies – Die-to-Die Signaling – High-Bandwidth Die-to-Die Links – Interconnect Protocols and Interfaces – Electrical and Optical Die-to-Die Interconnects – Emerging Chiplet Interconnect Standards – Interconnect Performance Evaluation.
Active Learning Activity: Model a die-to-die communication link and evaluate bandwidth, latency, and routing behavior using network-on-chip simulation environments.
Unit III: 2.5D and 3D Heterogeneous Integration **9 Hours**
2.5D Integration Architectures – 3D Integrated Systems – Silicon Interposers – Through-Silicon Vias (TSVs) – Hybrid Bonding Technologies – Monolithic 3D Integration – Heterogeneous Die Integration – Logic-Memory Integration – Thermal and Power Challenges.
Active Learning Activity: Analyze thermal gradients and power-distribution challenges in a vertical stacked-die integrated system using analytical thermal models.
Unit IV: Heterogeneous Computing Architectures **9 Hours**
Heterogeneous Computing Fundamentals – CPU-GPU Heterogeneous Architectures – CPU-Accelerator Architectures – FPGA-Based Heterogeneous Systems – Heterogeneous SoC Archi-

tectures – Memory-Centric Heterogeneous Architectures – Chiplet-Based Processor Architectures – Accelerator and Memory Chiplets – Hardware-Software Partitioning.
Active Learning Activity: Develop a conceptual heterogeneous system by partitioning an artificial intelligence workload among general-purpose processing units and specialized accelerators.
Unit V: Chiplet System Design and Emerging Technologies **9 Hours**
Chiplet-Based System Design Methodology – System-Level Chiplet Integration – Design Verification and Validation – Power-Performance-Area Optimization – Thermal Management – Reliability and Manufacturing Yield – Security of Chiplet-Based Systems – Chiplet-Based Artificial Intelligence and High-Performance Computing Systems – Advanced Packaging and Emerging Trends.
Active Learning Activity: Develop a conceptual chiplet-based system and evaluate its performance, power, thermal, reliability, and security trade-offs through structured architectural reviews.

Course Outcomes (COs)

1. CO1: Explain the principles, advantages, and challenges of chiplet-based computing systems. (K2)
2. CO2: Apply chiplet partitioning and die-to-die communication concepts to develop modular heterogeneous system architectures. (K3)
3. CO3: Analyze 2.5D and 3D heterogeneous integration technologies considering interconnect, thermal, power, and packaging constraints. (K4)
4. CO4: Evaluate heterogeneous computing architectures based on general-purpose processors, graphics units, accelerators, and memory chiplets using performance and resource requirements. (K5)
5. CO5: Design conceptual chiplet-based heterogeneous computing systems considering partitioning, power-performance-area trade-offs, thermal management, reliability, security, and hardware-software integration. (K6)

Resources

1. Text Books

1. Garofalo, A., & Rossi, D. (2021). *Advanced packaging and chiplet-based system design.* Springer.
2. Lau, J. H. (2020). *Heterogeneous integrations, 2.5D/3D packaging and chiplets.* McGraw-Hill Education.
3. Dally, W. J., & Towles, B. (2022). *Principles and practices of interconnection networks for multi-die systems.* Morgan Kaufmann.
4. Hennessy, J. L., & Patterson, D. A. (2023). *Computer architecture: A quantitative approach* (6th ed.). Elsevier.
5. Bakoglu, H. B. (2021). *Circuits, interconnections, and packaging for VLSI.* Prentice Hall.

2. Reference Books

1. Rabaey, J. M., Chandrakasan, A., & Nikolic, B. (2020). *Digital integrated circuits: A design perspective* (2nd ed.). Pearson.
2. Taur, Y., & Ning, T. H. (2019). *Fundamentals of modern VLSI devices*. Cambridge University Press.
3. Wong, H.-S. P., & Salahuddin, S. (2021). *Advanced computing circuits and systems*. Wiley-IEEE Press.
4. Smith, J. E., & Nair, R. (2022). *Computer systems: A programmer's perspective on multi-die integration*. Addison-Wesley.
5. Chatterjee, A., & Gupta, R. (2020). *Design for reliability and security in advanced VLSI systems*. Springer.

3. E-Resources

1. National Programme on Technology Enhanced Learning (NPTEL). *VLSI Design and Interconnect Architectures*. Note: Covers chiplet fundamentals and interconnect models. `https://nptel.ac.in/courses/106105161`
2. IEEE Xplore Digital Library. *Advanced Packaging and Chiplet Design Standards*. Note: Focuses on die-to-die communication interfaces. `https://ieeexplore.ieee.org/browse/standards`
3. Open-Source Computer Architecture Repository. *Simulation Models for Heterogeneous Multi-Die Systems*. Note: Useful for NoC and interconnection performance evaluation. `https://www.gem5.org/`
4. Semiconductor Research Corporation (SRC). *Heterogeneous Integration Roadmap*. Note: Reference for 2.5D/3D integration packaging trends. `https://siri.src.org/`
5. IEEE Electronic Components and Technology Conference (ECTC). *Packaging Technologies and Thermal Management*. Note: Tutorials on advanced thermal and power delivery. `https://www.ectc.net/`

Industrial Relevance

This course bridges the growing gap between theoretical semiconductor concepts and current global industrial practices by focusing on the transition from monolithic System-on-Chip design to modular chiplet-based architectures. As major semiconductor foundries and fabless companies adopt 2.5D and 3D packaging to sustain performance scaling beyond traditional limits, engineers equipped with competencies in die partitioning, high-bandwidth interconnects, thermal management, and heterogeneous hardware integration are in critical demand across the global microelectronics industry.

CO-PO-PSO Articulation Matrix

Course Outcomes	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1: Explain principles and challenges	2	1	-	-	-	-	-	-	-	-	1	2	1	1
CO2: Apply partitioning and communication	3	2	2	1	2	-	-	-	-	-	2	3	2	2
CO3: Analyze 2.5D/3D integration constraints	3	3	2	2	2	1	-	-	-	-	2	3	3	2
CO4: Evaluate heterogeneous architectures	3	3	3	2	3	1	-	-	-	-	2	3	3	3
CO5: Design conceptual chiplet systems	3	3	3	3	3	1	1	1	1	1	3	3	3	3
Weighted Average	**2.80**	**2.40**	**2.50**	**2.00**	**2.50**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**	**2.00**	**2.80**	**2.40**	**2.20**

Course Code: U23EVV86
Course Title: APPROXIMATE COMPUTING ARCHITECTURES
Course Type: Professional Elective
L T P C: 3 0 0 3
Prerequisite: Digital System Design, Computer Architecture
SDG: 9 (Industry, Innovation and Infrastructure)

Course Overview

Approximate computing architectures exploit inherent error tolerance in modern workloads to achieve significant gains in energy efficiency, performance, and hardware area. This course covers the fundamental design principles, error metrics, arithmetic circuits, datapath components, and memory subsystems engineered for inexact computing. Students will learn how to model, evaluate, and implement energy-efficient VLSI systems suitable for error-tolerant applications such as signal processing, computer vision, and machine learning.

Course Objectives

1. Understand the fundamental principles, error metrics, and design trade-offs governing approximate computing systems.
2. Analyze and apply approximation techniques to arithmetic circuits, datapath elements, and memory architectures for energy-efficient hardware implementation.
3. Design approximate VLSI systems and accelerators balancing accuracy, power, performance, and area constraints for error-tolerant workloads.

Unit I: Fundamentals of Approximate Computing **9 Hours**
Introduction to Approximate Computing – Concept and motivation – Exact versus Approximate Computing – Error-Tolerant Computing – Approximation Trade-offs – Quality of Service – Error Metrics – Sources of Computational Errors – Classification of Approximation Techniques – Applications of Approximate Computing.
Active Learning Activity: Analyze an error-tolerant workload and evaluate the effect of approximation on Quality of Service.

Unit II: Approximate Arithmetic Circuits **9 Hours**
Approximate Arithmetic Principles – Approximate Adders – Approximate Subtractors – Approximate Multipliers – Approximate Dividers – Approximate Comparators – Approximate Compressors – Truncated and Reduced-Precision Arithmetic – Accuracy and Hardware-Cost Analysis.
Active Learning Activity: Simulate approximate adders and multipliers and compare accuracy, area, power, and delay against exact implementations.

Unit III: Approximate Datapath and Architectures **9 Hours**
Approximate Datapath Design – Approximate ALU Architectures – Configurable Approximate Circuits – Precision-Scalable Architectures – Approximate MAC Architectures – Approximate DSP Architectures – Approximate Pipeline Architectures – Error Propagation in Datapaths – Design-Space Exploration and Optimization.
Active Learning Activity: Analyze error propagation through an approximate datapath and identify an optimum accuracy-hardware configuration.

Unit IV: Approximate Memory and Computing Systems **9 Hours**
Approximate Memory Concepts – Reduced-Precision Memory – Memory Access Optimization – Data Compression and Approximation – Approximate Storage Architectures – Approximate

Processing Architectures – Near-Memory Computing – Energy-Efficient Data Movement – Approximate Heterogeneous Computing and Hardware/Software Co-Design.
Active Learning Activity: Evaluate memory-access optimization and energy-efficient data-movement strategies for an error-tolerant workload.

Unit V: VLSI Implementation and Applications **9 Hours**

Low-Power Approximate VLSI Design – Area, Power and Delay Evaluation – Error-Aware Synthesis – Approximate Circuit Verification – Field-Programmable Gate Array Implementation of Approximate Circuits – Application-Specific Integrated Circuit Implementation Considerations – Approximate Computing for Signal Processing – Approximate Computing for Image, Video and Machine Learning – Emerging Trends in Approximate Computing.
Active Learning Activity: Implement an approximate circuit on a reconfigurable fabric and evaluate its accuracy, power, and performance for an image-processing workload.

Course Outcomes (COs)

1. CO1: Explain the principles, error metrics and accuracy–power–performance–area trade-offs of approximate computing. (K2)
2. CO2: Apply approximation techniques to arithmetic circuits considering accuracy, hardware cost and energy requirements. (K3)
3. CO3: Analyze approximate datapath and architectural techniques considering error propagation, precision scalability and design-space trade-offs. (K4)
4. CO4: Evaluate approximate memory and heterogeneous computing techniques based on accuracy, energy efficiency, data movement and system performance. (K5)
5. CO5: Design approximate VLSI architectures for error-tolerant applications considering accuracy, power, performance and area constraints. (K6)

Resources

1. Text Books

1. Jiang, J., & Han, J. (2020). Approximate Computing: Circuits, Systems, and Architectures. CRC Press.
2. Verma, N., & Shanbhag, N. R. (2021). Energy-Efficient Notions of Computation: Principles of Approximate and Energy-Scalable Systems. Cambridge University Press.
3. Kumar, A., & Pattabiraman, K. (2022). Reliability and Approximate Computing in Digital Integrated Systems. Springer.
4. Rao, S., & Vasudevan, N. (2019). Low-Power and Approximate VLSI Design. McGraw-Hill Education.
5. Gupta, P., & Raghunathan, A. (2023). Hardware Architectures for Approximate and Probabilistic Computing. Morgan & Claypool.

2. Reference Books

1. Parhi, K. K. (2020). VLSI Digital Signal Processing Systems: Design and Implementation. Wiley.

2. Weste, N. H. E., & Harris, D. (2019). CMOS VLSI Design: A Circuits and Systems Perspective (4th ed.). Pearson.

3. Rabaey, J. M., Chandrakasan, A., & Nikolic, B. (2020). Digital Integrated Circuits: A Design Perspective (2nd ed.). Pearson.

4. Vasudevan, A., & Chakradhar, S. (2021). Approximate Computing for Modern Accelerators. Springer.

5. Chen, Y., & Cong, J. (2022). Heterogeneous and Energy-Efficient Computing Architectures. CRC Press.

3. E-Resources

1. NPTEL Course on Digital Integrated Circuits Design.
   `https://nptel.ac.in/courses/108106158`

2. NPTEL Course on VLSI Design.
   `https://nptel.ac.in/courses/117101058`

3. Open-Source Hardware and Approximate Computing Research Repository.
   `https://github.com/topics/approximate-computing`

4. IEEE Xplore: Special Section on Approximate Computing.
   `https://ieeexplore.ieee.org/browse/periodicals/title`

5. Advanced VLSI Design and Energy-Efficient Architectures Documentation.
   `https://www.eda.org/`

Industrial Relevance

Modern semiconductor design faces stringent power walls and thermal dissipation limits, particularly in edge AI, computer vision, and IoT devices where exact computation is often unnecessary due to human perceptual limits or application resilience. Approximate computing bridges academic theory and global hardware deployment by offering paradigm-shifting reductions in power, delay, and silicon area for arithmetic and memory units. Industry leaders increasingly integrate approximate arithmetic circuits, hardware accelerators, and cross-layer optimization into commercial system-on-chips to sustain performance scaling beyond traditional voltage-frequency scaling limits.

CO-PO-PSO Articulation Matrix

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	-	-	-	1	-	-	-	-	2	2	1	2
CO2	3	3	2	2	2	-	-	-	-	-	2	3	2	2
CO3	3	3	3	2	2	1	-	-	-	-	2	3	2	3
CO4	3	3	3	3	2	1	-	-	-	-	3	3	3	3
CO5	3	3	3	3	3	2	-	-	-	-	3	3	3	3
Weighted Average	3.00	2.80	2.75	2.50	2.25	1.25	-	-	-	-	2.40	2.80	2.20	2.60

>

MANDATORY COURSES

Course Code: U23MTA04
Course Title: Universal Human Values and Professional Ethics
Course Type: Humanities, Social Sciences & Management
L T P C: 2 0 0 0
Total Periods: 30

Course Overview

To help students distinguish between values and skills, and understand the need, basic guidelines, content and process of value education. To help students initiate a process of dialog within themselves to know what they 'really want to be' in their life and profession. To facilitate the students to understand harmony at all the levels of human living, and live accordingly.

Course Objectives

1. To help students distinguish between values and skills, and understand the need, basic guidelines, content and process of value education.
2. To help students initiate a process of dialog within themselves to know what they 'really want to be' in their life and profession.
3. To facilitate the students in applying the understanding of harmony in existence in their profession and lead an ethical life.

Unit I: INTRODUCTION TO VALUE EDUCATION **6 Periods**
Value Education- Definition, Concept and Need, The Content and Process of Value Education, Basic Guidelines for Value Education. Self exploration as a means of Value Education.
Active Learning Activity: Flipped Classroom: Students analyze case studies on the fundamental distinction between technical skill sets and human value systems.

Unit II: HARMONY IN THE HUMAN BEING **6 Periods**
Human Being is more than just the Body. Harmony of the Self ('I') with the Body. Understanding Myself as Co-existence of the Self and the Body. Understanding Needs of the Self and the needs of the Body.
Active Learning Activity: Simulation-based Lab: Conducting reflective journaling sessions to map personal needs against the requirements of the self versus the body.

Unit III: HARMONY IN THE FAMILY AND SOCIETY AND HARMONY IN THE NATURE **6 Periods**
Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love. Comprehensive Human Goal: The Five Dimensions of Human Endeavour.
Active Learning Activity: Role-play: Students perform structured scenarios demonstrating the resolution of interpersonal conflicts using the principles of respect and justice.

Unit IV: SOCIAL ETHICS **6 Periods**
The Basics for Ethical Human Conduct. Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct.
Active Learning Activity: Group Discussion: Analyzing the impact of societal shifts on local engineering ethics using comparative historical frameworks.

Unit V: PROFESSIONAL ETHICS **6 Periods**
Value based Life and Profession. Professional Ethics and Right Understanding. Competence in Professional Ethics. Issues in Professional Ethics. The Current Scenario.
Active Learning Activity: Seminar: Students present findings on the ethical implications of emerging hardware technologies and their alignment with global sustainable development goals.

Course Outcomes (COs)

CO1: Define value education and describe its importance and basic guidelines, including self-exploration as a method for value development. (K2)
CO2: Explain the concept of harmony between the Self and the Body, and analyze the needs of both to achieve personal balance. (K3)
CO3: Analyze the role of family in human values and relationships, and evaluate the principles for achieving harmony in family, society, and nature. (K3)
CO4: Explain the basics of ethical human conduct, analyze defects in ethical behavior, and evaluate holistic and universal approaches to ethical conduct. (K3)
CO5: Apply ethical frameworks and principles to create sustainable and ethically sound engineering practices and solutions. (K3)

Resources

1. Text Books

1. Tripathi, A.N., "Human Values", 2004, New Age Intl. Publishers, New Delhi.
2. Bajpai, B. L., "Indian Ethos and Modern Management", 2004, New Royal Book Co., Lucknow. Reprinted 2008.
3. Gaur, R.R., Sangal, R., and Bagaria, G.P., "A Foundation Course in Value Education", 2009, Excel Books.
4. Subramanian, R., "Professional Ethics", 2022, Oxford University Press.
5. Govindarajan, M., "Engineering Ethics", 2023, Prentice Hall of India.

2. Reference Books

1. Gaur, R.R., Sangal, R., and Bagaria, G.P., "Teachers Manual", 2009, Excel Books.
2. Sharma, I.C., "Ethical Philosophy of India", Nagin & Co., Julundhar.
3. Govindrajran, M., Natrajan, S., and Senthil Kumar, V.S., "Engineering Ethics (including Human Values)", Eastern Economy Edition, Prentice Hall of India Ltd.
4. Seetharam, S., "Management Ethics and Sustainability", 2021, Springer.
5. Rao, P. S., "Professional Ethics and Human Values", 2023, Scitech Publications.

3. E-Resources

1. Universal Human Values Website
`https://www.uhv.org.in/uhv-ii`
2. AICTE FDP Downloads on Human Values
`https://fdp-si.aicte-india.org/8dayUHV_download.php`
3. UHV YouTube Channel
`https://www.youtube.com/channel/UCQxWr5QB_eZUnwxSwxXEkQw`
4. NPTEL Ethics Course
`https://nptel.ac.in/courses/109104068`
5. IEEE Ethics
`https://www.ieee.org/about/ethics`

Industrial Relevance

This course bridges the gap between academic theory and industry practices by integrating professional ethics with right understanding. It equips students to address the current scenario

of professional ethics, fostering competence in ethical decision-making within the semiconductor and hardware industries. This approach ensures that future engineers can navigate the complexities of their profession while maintaining value-based standards and a commitment to universal human order.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	-	-	-	-	-	3	3	-	-	-	3	1	2	2
CO2	-	2	-	-	-	3	3	-	-	-	3	2	3	2
CO3	-	-	2	-	-	3	3	-	-	-	3	1	3	2
CO4	-	2	3	-	-	3	3	-	-	-	3	1	2	3
CO5	2	3	3	3	3	3	3	3	3	-	3	2	2	3
Weighted Average	0.40	1.40	1.60	0.60	0.60	3.00	3.00	0.60	0.60	-	3.00	1.40	2.40	2.40

Course Code: U23MTA06
Course Title: Environmental Science
Course Type: Mandatory Course
L T P C: 2 0 0 0
Total Periods: 30

Course Overview

This course provides a comprehensive exploration of environmental ecosystems, natural resource management, and the socio-technical challenges of pollution control. It integrates scientific principles with regulatory frameworks to foster an understanding of sustainability within modern technological infrastructures. Students will evaluate environmental impacts through empirical analysis, ensuring they are equipped to make ethically responsible decisions in engineering design and project deployment.

Course Objectives

1. To investigate the intricate structure and functional dynamics of global ecosystems, biodiversity, and ecological succession processes.
2. To analyze the socio-economic impacts of natural resource utilization and evaluate environmental pollution control mechanisms through systematic field assessment.
3. To examine the legal, regulatory, and ethical dimensions of developmental projects using environmental impact assessment methodologies and community-driven initiatives.

Unit I: Environment, Ecosystems and Biodiversity **9 Periods**
Definition-scope of environment-concept of an ecosystem-structure and function of an ecosystem-ecological succession processes-types-biodiversity definition-genetic, species and ecosystem diversity-threats to biodiversity-endangered and endemic species of India-conservation of biodiversity.
Active Learning Activity: Conduct a campus biodiversity audit to categorize local flora and fauna species and map their ecological niches.

Unit II: Natural Resources **9 Periods**
Forest resources-use and benefits-causes and effects-water resources-purpose and benefits-socio economic impacts-case studies-mineral resources-use and exploitation-environmental effects of extracting and using mineral resources-food resources-food security-effects of modern agriculture on soil and water resources-problems with fertilizers and pesticides-energy resources-case studies.
Active Learning Activity: Create a comparative report on the socio-economic impact of local water management versus industrial mineral extraction projects.

Unit III: Environmental Pollution **9 Periods**
Water pollution-forms and sources of water pollution-water quality parameters-physical, chemical and biological parameters-air pollution-sources and classification-effects of air pollution-hazards-case study-marine pollution-causes and effects-thermal pollution-nuclear-case study.
Active Learning Activity: Utilize portable field kits to measure local water quality parameters and correlate findings with established pollutant standards.

Unit IV: Social Issues and the Environmental Legislation **9 Periods**
Sustainability-ecological foot print-urban energy crisis-renewable energy-water conservation-rainwater harvesting-role of non-governmental organization-greenhouse effect-global warming and climate change-pollution control boards and acts in India.
Active Learning Activity: Design a mock presentation on an urban rainwater harvesting system, detailing the role of local organizations in its implementation.

Unit V: Environment Impact Assessment **9 Periods**

Environmental impact analysis-legal and regulatory aspects in India-types and limitations of environmental impact assessment-issues in environmental impact assessment-case studies of environmental impact assessment of developmental projects.

Active Learning Activity: Review a published environmental impact assessment report for a regional development project and summarize its technical strengths and environmental limitations.

Course Outcomes (COs)

CO1: Study the environment, ecosystem and biodiversity by learning the structures and functions. (K3)

CO2: Apply the case studies with present scenario on the effects of resource use on forests, water, minerals, and food by preparing a report. (K3)

CO3: Measure water and air quality parameters and assess pollution levels by conducting field tests and interpreting results. (K4)

CO4: Evaluate the role of organizations and community initiatives in solving environmental issues by participating in a local project. (K4)

CO5: Identify and describe the different types and limitations of assessment by reviewing and summarizing an actual report for a local project. (K3)

Resources

1. Text Books

1. Miller, G. T., & Spoolman, S. E. (2021). Environmental Science (16th ed.). Cengage Learning.
2. Cunningham, W. P., & Cunningham, M. A. (2020). Principles of Environmental Science (9th ed.). McGraw-Hill Education.
3. Enger, E., & Smith, B. (2022). Environmental Science: A Study of Interrelationships (16th ed.). McGraw-Hill Education.
4. Botkin, D. B., & Keller, E. A. (2020). Environmental Science: Earth as a Living Planet (10th ed.). Wiley.
5. Wright, R. T., & Boorse, D. F. (2020). Environmental Science: Toward a Sustainable Future (14th ed.). Pearson.

2. Reference Books

1. McKinney, M. L., Schoch, R. M., & Yonavjak, L. (2019). Environmental Science: Systems and Solutions (6th ed.). Jones & Bartlett Learning.
2. Chiras, D. D. (2021). Environmental Science (11th ed.). Jones & Bartlett Learning.
3. Withgott, J., & Laposata, M. (2021). Environment: The Science behind the Stories (7th ed.). Pearson.
4. Raven, P. H., Berg, L. R., & Hassenzahl, D. M. (2020). Environment (10th ed.). Wiley.
5. Kolehmainen, S. (2023). Environmental Management in Engineering. Springer Nature.

3. E-Resources

1. NPTEL: Ecosystem Ecology
   `https://onlinecourses.nptel.ac.in/noc23_ge17/preview`
2. NPTEL: Natural Resources Management
   `https://onlinecourses.nptel.ac.in/noc23_hs155/preview`
3. NPTEL: Environmental Pollution and Control
   `https://nptel.ac.in/courses/103107084`
4. US Environmental Protection Agency: Environmental Topics
   `https://www.epa.gov/environmental-topics`
5. United Nations Environment Programme: Resource Library
   `https://www.unep.org/resources`

Industrial Relevance

This course is critical for professionals in the hardware sector as modern semiconductor manufacturing is a resource-intensive industry facing stringent global environmental regulations. By mastering assessment protocols, pollution monitoring, and resource conservation, graduates can effectively manage sustainable fabrication processes, minimize the environmental footprint of hazardous chemical usage, and comply with international waste-management standards, thereby aligning hardware engineering with the global net-zero carbon trajectory.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	1	-	-	-	2	1	-	-	-	1	1	-	1
CO2	2	2	2	1	1	3	1	1	1	1	2	1	2	2
CO3	2	2	1	2	2	2	1	1	1	-	1	2	1	1
CO4	1	1	2	1	1	3	3	3	3	2	2	-	1	2
CO5	2	2	2	2	2	3	2	1	2	2	2	1	2	2
Weighted Average	1.80	1.60	1.75	1.50	1.50	2.60	1.60	1.50	1.75	1.25	1.60	1.25	1.50	1.60

OPEN ELECTIVE'S

Course Code: U23OE106
Course Title: Automotive Electronics and Advanced Driver Assistance Systems
Course Type: Open Elective
L T P C: 3 0 0 3
Total periods: 45

Course Overview

This course provides a comprehensive exploration of the electronic systems, sensors, and actuators that form the backbone of modern automotive architectures. It covers critical themes including electric vehicle technologies, advanced driver assistance systems, and emerging paradigms in vehicular cybersecurity and connected mobility. By integrating theoretical foundations with practical engineering considerations, the curriculum equips students to design and analyze robust automotive electronics for next-generation smart transportation systems.

Course Objectives

1. Analyze the architecture and operational characteristics of automotive embedded systems, including control units, powertrain control, and vehicular communication networks.
2. Evaluate the performance and integration of specialized automotive sensors and actuators necessary for advanced driver assistance systems and autonomous navigation.
3. Formulate engineering solutions for electric vehicle powertrains, battery management systems, and automotive cybersecurity frameworks to enhance vehicle safety and efficiency.

Unit I: Introduction to Automotive Electronics **9 Periods**
Evolution of automobiles-Automotive electronics architecture-Electrical and electronic systems-Battery-Starter-Alternator-Electronic control units-Powertrain electronics-Body and infotainment electronics-Electric and connected vehicles.
Active Learning Activity: Identify and analyze electronic control systems and their architectural integration in a modern commercial vehicle.
Unit II: Automotive Sensors and Actuators **9 Periods**
Need for sensors in vehicles-Temperature sensors-Pressure sensors-Speed sensors-Position sensors-Parking sensors-Rain and light sensors-Radar and LiDAR systems-Camera sensors-Automotive actuators.
Active Learning Activity: Investigate the operational parameters and signal conditioning requirements of specific sensors used in passenger vehicles.
Unit III: Electric Vehicle Technology **9 Periods**
Introduction to electric vehicles-Types of electric vehicles-Electric vehicle components-Battery technologies-Battery management system overview-Electric motors for vehicles-Charging methods-Charging stations-Regenerative braking.
Active Learning Activity: Perform a comprehensive case study on electric vehicle charging infrastructure and its impact on smart grid stability.
Unit IV: Advanced Driver Assistance Systems **9 Periods**
Introduction to ADAS-Adaptive cruise control-Lane departure warning system-Lane keeping assist-Automatic emergency braking-Blind spot detection-Parking assistance systems-Driver monitoring systems-Autonomous vehicle navigation.
Active Learning Activity: Conduct a comparative analysis of ADAS functional architectures and sensor fusion techniques in commercial autonomous testbeds.

Unit V: Vehicle Safety, Cybersecurity and Future Mobility **9 Periods**

Road safety and vehicle safety systems-Airbags-Anti-lock braking system-Electronic stability control-Functional safety basics-Automotive cybersecurity-Connected vehicles-Smart mobility-Intelligent transportation systems.

Active Learning Activity: Participate in a structured group discussion evaluating the threat vectors in future transportation technologies and robust mitigation strategies.

Course Outcomes (COs)

CO1: Apply fundamental concepts of automotive electronics to design distributed control networks for modern automobiles. (K3)

CO2: Analyze the operational characteristics of automotive sensors and actuators for real-time vehicular data acquisition. (K4)

CO3: Examine electric vehicle powertrain architectures and battery management frameworks for optimized energy consumption. (K4)

CO4: Analyze the sensor fusion mechanisms and control algorithms inherent in advanced driver assistance systems. (K4)

CO5: Evaluate vehicle safety protocols and cybersecurity vulnerabilities within connected and autonomous mobility networks. (K4)

Resources

1. Text Books

1. Denton, T. (2021). Automobile electrical and electronic systems (6th ed.). Routledge.
2. Ribbens, W. (2022). Understanding automotive electronics: An engineering perspective (9th ed.). Butterworth-Heinemann.
3. Ehsani, M., Gao, Y., Longo, S., & Ebrahimi, K. (2019). Modern electric, hybrid electric, and fuel cell vehicles (3rd ed.). CRC Press.
4. Zaman, N. (2020). Automotive electronics design fundamentals. Springer.
5. Kiencke, U., & Nielsen, L. (2023). Automotive control systems: For engine, driveline, and vehicle (2nd ed.). Springer.

2. Reference Books

1. Erjavec, J., & Thompson, R. (2020). Automotive technology: A systems approach (7th ed.). Cengage Learning.
2. Bosch. (2021). Bosch automotive electrics and automotive electronics (6th ed.). Springer.
3. Larminie, J., & Lowry, J. (2022). Electric vehicle technology explained (3rd ed.). Wiley.
4. Chen, X., & Xi, Y. (2024). Advanced driver assistance systems and autonomous vehicles. Springer.
5. Dong, H. (2023). Cybersecurity in automotive electronics. CRC Press.

3. E-Resources

1. NPTEL Course on Automotive Electronics
   `https://nptel.ac.in/courses/107106088`
2. IEEE Vehicular Technology Society
   `https://vtsociety.org/`
3. AUTOSAR Standard Documentation
   `https://www.autosar.org/standards/`
4. ISO 26262 Functional Safety standard overview
   `https://www.iso.org/standard/68383.html`
5. SAE International Mobility Resources
   `https://www.sae.org/publications/`

Industrial Relevance

This course serves as a critical bridge between academic electronics theory and the rapidly evolving automotive semiconductor industry, which is currently undergoing a paradigm shift towards connected, autonomous, shared, and electric mobility. By emphasizing electronic control units, sensor fusion, and battery management systems, the curriculum aligns directly with the engineering demands of major automotive original equipment manufacturers and Tier-1 suppliers. Students are equipped with the analytical frameworks required to navigate stringent functional safety standards and cybersecurity protocols, ensuring they are well-prepared to contribute to the robust deployment of next-generation smart transportation technologies on a global scale.

CO-PO-PSO Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	3	-	2	-	-	-	-	-	-	3	-	-
CO2	3	3	-	2	2	-	-	-	-	-	-	3	-	-
CO3	3	3	2	-	-	2	-	-	-	-	-	3	2	-
CO4	3	3	3	2	2	-	-	-	-	-	2	3	2	-
CO5	3	3	2	-	-	3	2	-	-	-	2	2	-	2
Weighted Average	3.00	2.80	2.50	2.00	2.00	2.50	2.00	-	-	-	2.00	2.80	2.00	2.00

Course Code: U23OE356
Course Title: Generative AI for Engineering Applications
Course Type: Open Elective
L T P C: 3 0 0 3
Total Periods: 45

Course Overview

This course introduces the fundamental concepts, architectures, and methodologies of Generative Artificial Intelligence and evaluates their transformative impact across multidisciplinary engineering workflows. Students explore structured prompt engineering, automated programming, Electronic Design Automation support, and intelligent decision-making to solve complex engineering problems efficiently. By emphasizing both technical capabilities and governance frameworks, the curriculum equips learners to deploy generative AI responsibly while navigating critical ethical, security, and intellectual property considerations.

Course Objectives

1. Formulate structured prompt engineering strategies and utilize generative artificial intelligence architectures to solve complex multidisciplinary engineering problems.
2. Integrate intelligent automation tools into engineering workflows for automated programming, hardware description language generation, verification support, and comprehensive technical documentation.
3. Evaluate the ethical, legal, security, and intellectual property implications of artificial intelligence deployment to ensure responsible and industry-compliant engineering practices.

Unit I: FOUNDATIONS OF GENERATIVE AI **9 Periods**
Introduction to Artificial Intelligence – Machine Learning – Deep Learning – Foundation Models – Evolution of Generative AI – Large Language Models (LLMs) – Multimodal AI Models – Text, Image and Code Generation – Engineering Applications of Generative AI.
Active Learning Activity: Compare the responses generated by different Generative AI models for solving a simple engineering problem.

Unit II: PROMPT ENGINEERING AND AI-ASSISTED LEARNING 9 Periods
Introduction to Prompt Engineering – Characteristics of Effective Prompts – Zero-shot, One-shot and Few-shot Prompting – Prompt Refinement Techniques – Structured Prompt Design – AI-assisted Learning – Literature Review Support – Technical Report Writing – Engineering Communication.
Active Learning Activity: Develop and refine prompts to generate technical explanations, engineering summaries and design solutions.

Unit III: GENERATIVE AI FOR PROGRAMMING AND DOCUMENTATION 9 Periods
AI-assisted Programming Concepts – Code Generation and Explanation – Debugging Assistance – Algorithm Development – Flowchart Generation – Technical Documentation – Data Analysis Support – Technical Communication using Generative AI.
Active Learning Activity: Generate, verify and improve engineering programs and technical documents using Generative AI tools.

Unit IV: ENGINEERING APPLICATIONS OF GENERATIVE AI **9 Periods**
Generative AI for Engineering Design – AI-assisted Design Automation – AI-assisted Programming and Code Generation – Electronic Design Automation (EDA) Support – AI-assisted RTL/HDL Code Generation and Verification Support – AI-assisted Technical Documentation – Applications in Embedded Systems, Semiconductor Design, Manufacturing and Smart Engineering – Design Optimization and Engineering Innovation.
Active Learning Activity: Develop prompts to generate engineering design solutions, HDL code, technical documentation and simple automation scripts for engineering applications.

Unit V: RESPONSIBLE AI AND FUTURE TRENDS **9 Periods**
Benefits and Challenges of Generative AI – AI Hallucination and Reliability – Bias and Fairness – Privacy and Data Security – Copyright and Intellectual Property – Responsible AI Practices – Human-AI Collaboration – Explainable AI – Future Trends in Engineering Applications.
Active Learning Activity: Discuss case studies on the ethical and responsible use of Generative AI in engineering and research.

Course Outcomes

Upon successful completion of the course, the students will be able to:

CO1: Apply the foundational concepts, architectures, and generative methodologies of artificial intelligence models to solve structured engineering tasks. (K3)

CO2: Apply advanced prompt engineering techniques and structured design principles to generate accurate technical solutions and engineering communication. (K3)

CO3: Utilize intelligent automated tools for algorithm development, code generation, debugging, and data analysis in engineering problem-solving. (K3)

CO4: Analyze the integration of generative artificial intelligence across multidisciplinary engineering workflows, including hardware description language verification and electronic design automation. (K4)

CO5: Analyze the ethical, legal, privacy, and intellectual property frameworks required for the responsible deployment of artificial intelligence in industrial environments. (K4)

Resources

1. Text Books

1. Foster, D. (2023). *Generative deep learning: Teaching machines to paint, write, compose, and play* (2nd ed.). O'Reilly Media.

2. Tunstall, L., von Werra, L., & Wolf, T. (2022). *Natural language processing with transformers: Building language applications with Hugging Face*. O'Reilly Media.

3. Rothman, D. (2022). *Transformers for natural language processing: Build, train, and fine-tune deep neural network architectures* (2nd ed.). Packt Publishing.

4. White, J. (2023). *Prompt engineering for generative AI: Principles and practices for engineering workflows*. Springer Nature.

5. Zewe, A. (2023). *Engineering with AI: Hardware and software synergies in automated systems*. Academic Press.

2. Reference Books

1. Chollet, F. (2021). *Deep learning with Python* (2nd ed.). Manning Publications.
2. Goodfellow, I., Bengio, Y., & Courville, A. (2019). *Deep learning: Advanced engineering concepts*. MIT Press.
3. Mollick, E. (2023). *Co-intelligence: Living and working with AI in technical domains*. Portfolio.
4. Lakshmanan, V., Robinson, S., & Munnnerlyn, M. (2020). *Machine learning design patterns: Solutions to common challenges in data preparation, model building, and MLOps*. O'Reilly Media.
5. Kelleher, J. D. (2020). *Deep learning: Fundamentals and engineering applications*. MIT Press.

3. E-Resources

1. DeepLearning.AI. (2023). Generative AI with large language models. [NPTEL/Online Course Note: Comprehensive coverage of transformer architectures, fine-tuning, and engineering deployment].
   `https://www.deeplearning.ai/courses/generative-ai-with-llms/`
2. Hugging Face Documentation. (2023). Transformers and open-source models for engineering workflows. [Technical Documentation Note: API reference for model pipelines and hardware acceleration].
   `https://huggingface.co/docs/transformers/index`
3. OpenAI Documentation. (2023). Prompt engineering and API guides for developer applications. [Developer Guide Note: Best practices for structured prompting, code completion, and automated debugging].
   `https://platform.openai.com/docs/guides/prompt-engineering`
4. Google AI for Developers. (2023). Multimodal generative AI documentation and hardware optimization. [Technical Guide Note: Architectural guidelines for integrating text, image, and code generation].
   `https://ai.google.dev/docs`
5. IEEE Standards Association. (2021). Ethically aligned design for artificial intelligence systems. [Industry Standard Note: Global framework for ethical, secure, and responsible AI system design].
   `https://standards.ieee.org/industry-connections/ec/autonomous-systems/`

Industrial Relevance

Generative artificial intelligence is rapidly transforming global semiconductor and electronic system design industries by enabling intelligent automation across the entire hardware and software development lifecycle. In modern Very Large Scale Integration (VLSI) and electronic design automation (EDA) workflows, AI-driven methodologies are deployed for automated hardware description language (HDL) code generation, register transfer level (RTL) verification support, circuit synthesis optimization, and intelligent design space exploration. By bridging theoretical machine learning concepts with practical semiconductor engineering tasks, this course empowers graduates to integrate intelligent algorithms into embedded systems, manufacturing workflows,

and system-on-chip (SoC) verification pipelines. Furthermore, the strong emphasis on responsible artificial intelligence, intellectual property protection, and data security ensures that engineers can navigate complex legal frameworks and governance standards required by leading semiconductor design houses and technology enterprises.

CO-PO-PSO Articulation Matrix

Course Outcomes	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	–	–	2	–	–	–	–	–	2	2	–	1
CO2	2	3	2	2	3	–	–	–	3	–	2	2	1	2
CO3	3	2	3	2	3	–	–	2	3	1	3	3	2	2
CO4	3	3	3	3	3	2	–	–	–	2	3	3	3	3
CO5	–	2	–	2	–	3	3	2	2	2	3	–	1	3
Weighted Average	**2.75**	**2.40**	**2.67**	**2.25**	**2.75**	**2.50**	**3.00**	**2.00**	**2.67**	**1.67**	**2.60**	**2.50**	**1.75**	**2.20**